GDSS-MBB-87-001

AC Power System Breadboard

Final Report

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GENERAL DYNAMICS
Space Systems Division

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16. Abstract

The object of this program was to design, build, test, and deliver a high frequency (20-kHz) Power System Breadboard which would electrically approximate a pair of dual redundant power channels of an IOC Space Station. This report describes that program, including the technical background, and discusses the results, showing that the major assumptions about the characteristics of this class of hardware (size, mass, efficiency, control. etc.) were substantially correct. This testbed equipment has been completed and delivered to LeRC, where it is operating as a part of the Space Station Power System Test Facility.

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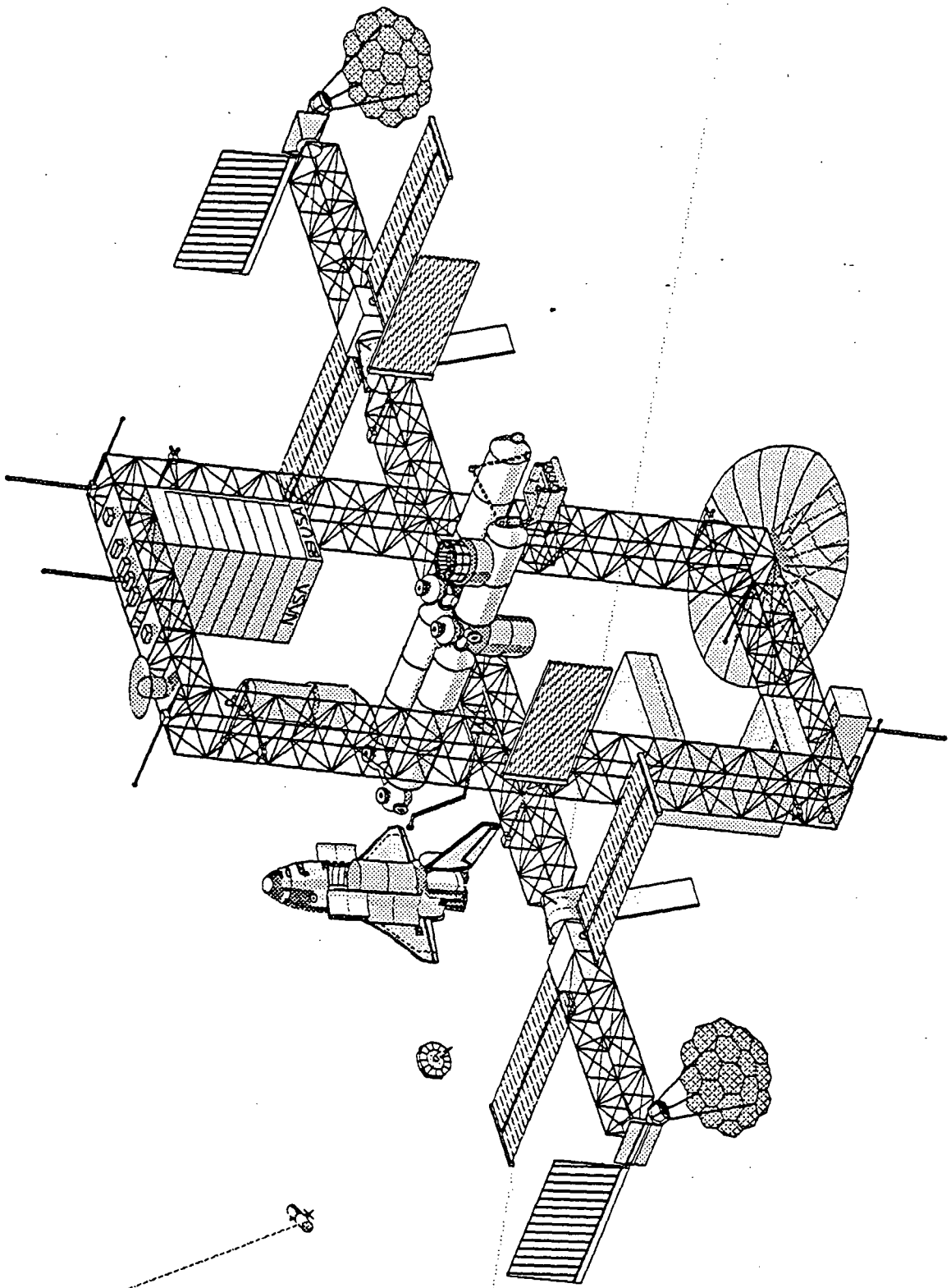

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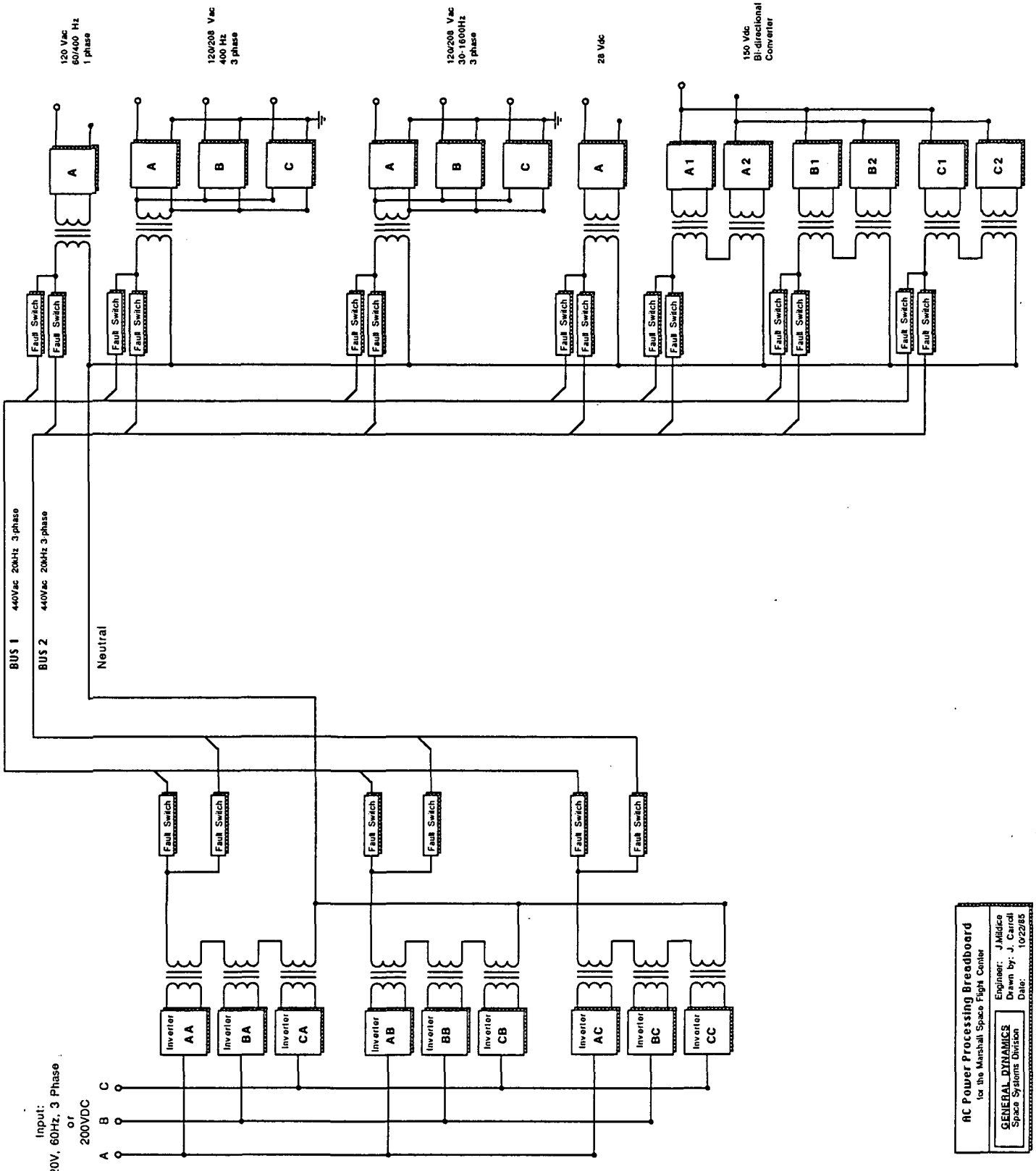

1.0 Summary

The objective of this program was to design, build, and deliver a high-frequency (20 kHz) Power System Breadboard which would electrically approximate a scaled-down (5 kW) version of the dual, redundant power channels of an IOC Space Station. A block diagram of that breadboard is shown in Figure 1-1, and includes the following major elements:

- Nine Inverter/Driver modules, which can be operated in single or three-phase mode, to test and demonstrate the hardware required to interface DC sources (solar arrays) or AC sources (turbo alternators) to the high frequency transmission bus system. They also act as the 20-kHz power sources to test other system components.

- A set of source control switches (analagous to the Space Station Remote Power Controllers or RPCs) to demonstrate autonomous system fault protection.

- A dual 50-meter transmission bus system.

- A set of load control switches (Remote Power Controllers) to show how the system will protect itself against load/user faults.

- A typical set of five high-power, user-interface units to investigate and define the best techniques to interface with DC loads, low-frequency AC loads, and energy storage devices such as batteries.

- A computer control system, including a Macintosh™ terminal and supervisory interface, which commands embedded processors in the power hardware, to demonstrate system control and computer interface designs. The control and interface designs use technologies appropriate for actual Space Station hardware.

The design approach was to use "Mapham"-derived (Reference 1) series-resonant, thyristor-switched, inverter/converter configurations of the type successfully designed and demonstrated by General Dynamics. New power stages are integrated with a previously developed set of control modules, (NAS 3-23878, Reference 2) to construct the family of power processors required.

The hardware constructed and delivered is intended to be an electrical analog of a possible flight configuration, but the mechanical design is appropriate to the laboratory environment, and is not representative of spacecraft configurations. Bus lengths (50 meters) and losses for power

transmission testing approximate worst cases expected on the current Space Station configuration. This provides high-fidelity hardware modeling of an area that has traditionally been difficult to model with analytical techniques.

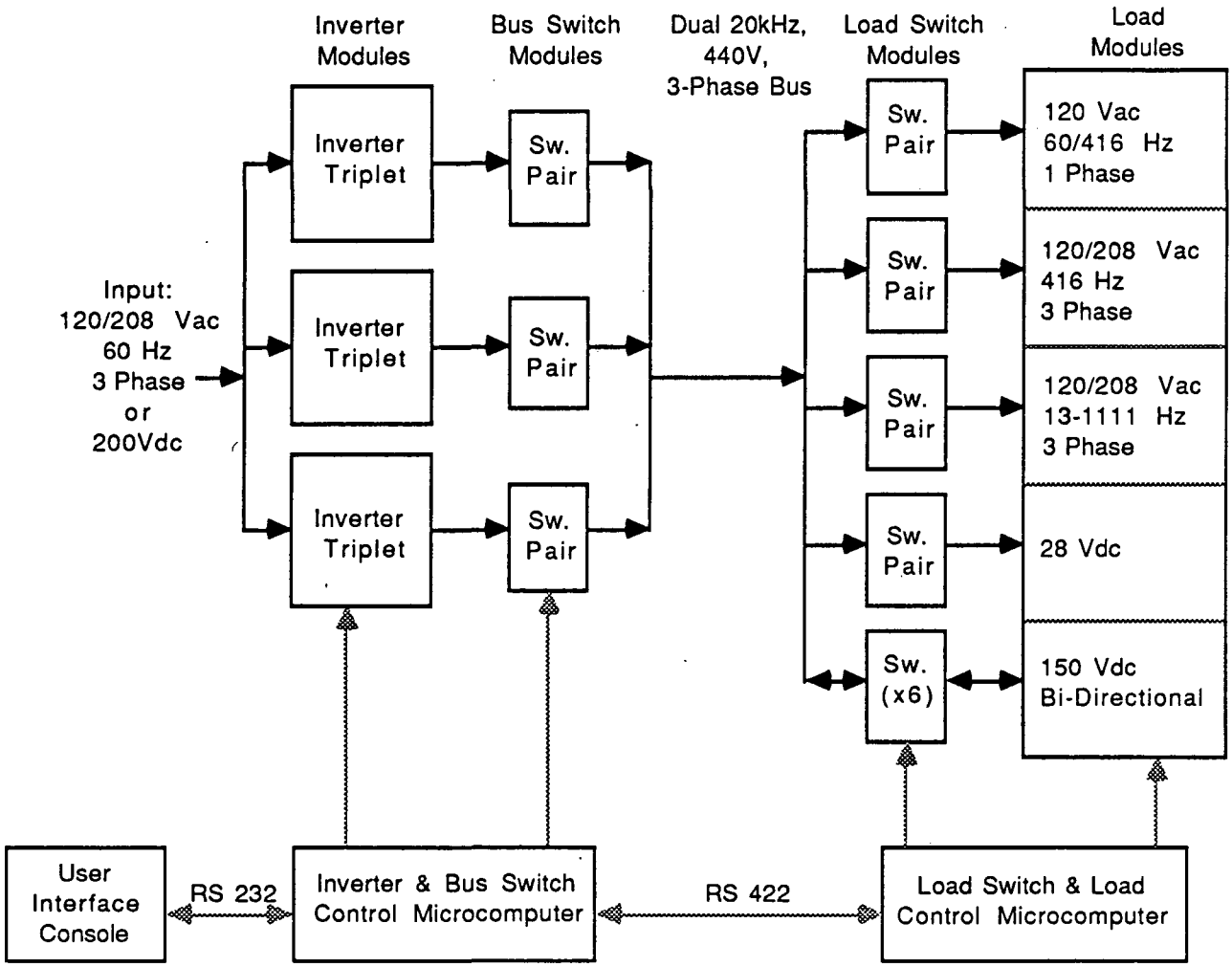

Figure 1-1. This high-level block diagram shows inverter modules, switch modules, transmission busses, load converter modules, and the control computers.

The test procedure was designed to demonstrate that the complete, integrated set of hardware operated properly and performed its basic design functions.

Finally, the completed, tested hardware was delivered to the NASA Marshall Space Flight Center, where it has been installed and tested in their facility.

Contract Overview:

- **Overall Goal:** Construct a 20-kHz power system breadboard representative of Space Station functions.

- **Contract Value:** $298K

- **Schedule:** Contract Start Date - May, 1985
  Hardware delivery - December, 1987

- **System Elements:**
  - Driver/Inverter Modules
  - Bus Control Switch Matrix
  - Power Bus
  - Load Control Switch Matrix
  - Variable-Voltage DC Receiver Module
  - Variable-Voltage, Variable-Frequency AC Receiver Modules
  - Bidirectional Converter Receiver Module
  - Computer/System Controller and Software

2.0 Introduction and Background

2.1 Theory of Operation

The high-frequency power system technology addressed by this program generates the basic AC transmission link power by exciting an underdamped, series-resonant, L-C circuit. The power bus therefore becomes an integral part of the resonant link in the more-or-less usual resonant converter configuration. The load-interface modules form the output stages. Therefore the power system for a vehicle is really one large, integrated, multiple-module resonant converter. Its range of properly underdamped operation is defined by the full load and no load system specifications.

While the basic configuration is a series-resonant design, it is not the familiar "Schwarz" (Reference 5) type. This design places the load (reflected through the output transformer) in parallel with the resonant capacitor in the method proposed by Neville Mapham (Reference 1). Figures 2-1 and 2-2 show the two circuit approaches.

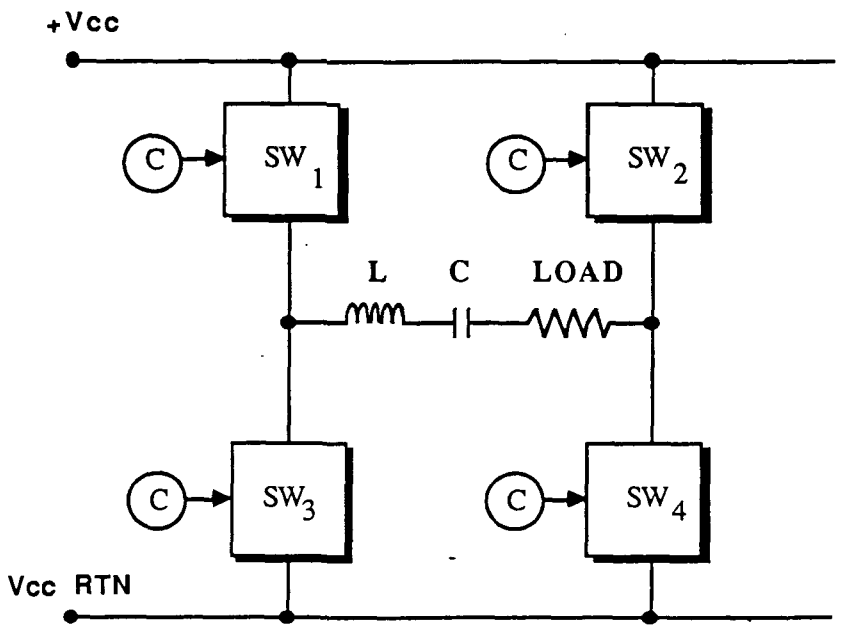

Figure 2-1. The Schwarz configuration has the load in series with the resonant circuit..

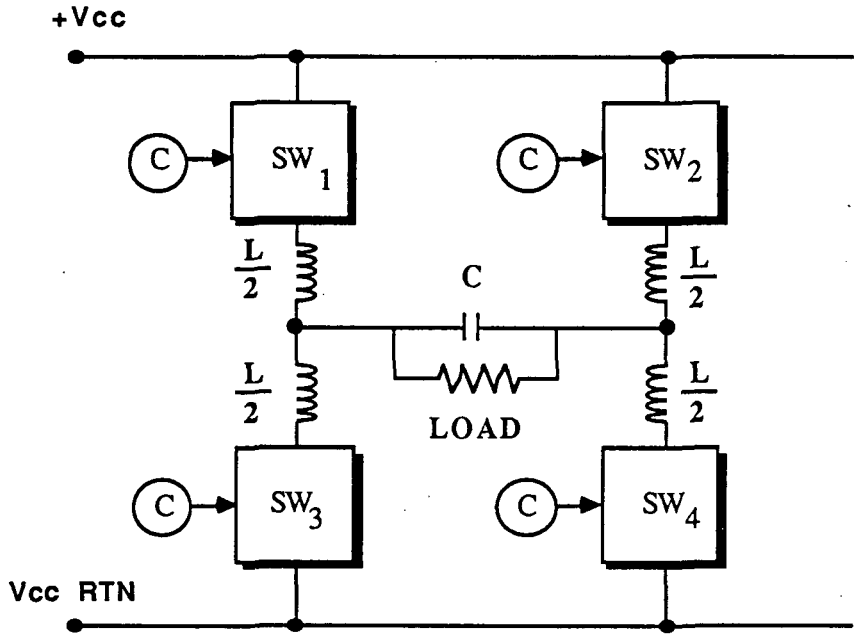

Figure 2-2. The Mapham circuit has the load in parallel with the resonant capacitor.

This gives us a system driver (inverter) that is essentially a voltage source as compared to the more usual "Schwarz" current source. This has obvious advantages for a power system. The line voltage is independent of the load (on a first order basis) and is tolerant of open circuits—obvious requirements for a utility system. In addition, the output frequency is clock controlled, and independent of variations in the resonant circuit components. This is a significant development for this class of hardware.

The basic power output hardware configuration for a single driver is shown in Figure 2-3. Two or more such drivers are arranged in series, with different phase shifts between one another, to add and provide power output closed-loop regulation. (See Figure 2-4.) The control circuits noted (c) in the above figures are the subject of the contract described in section 2.2.

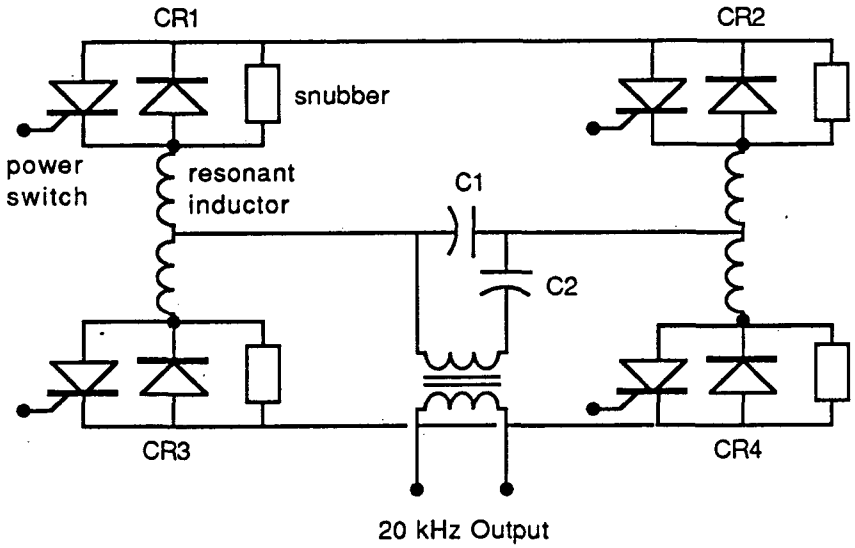

Figure 2-3. Basic Inverter Power Stage

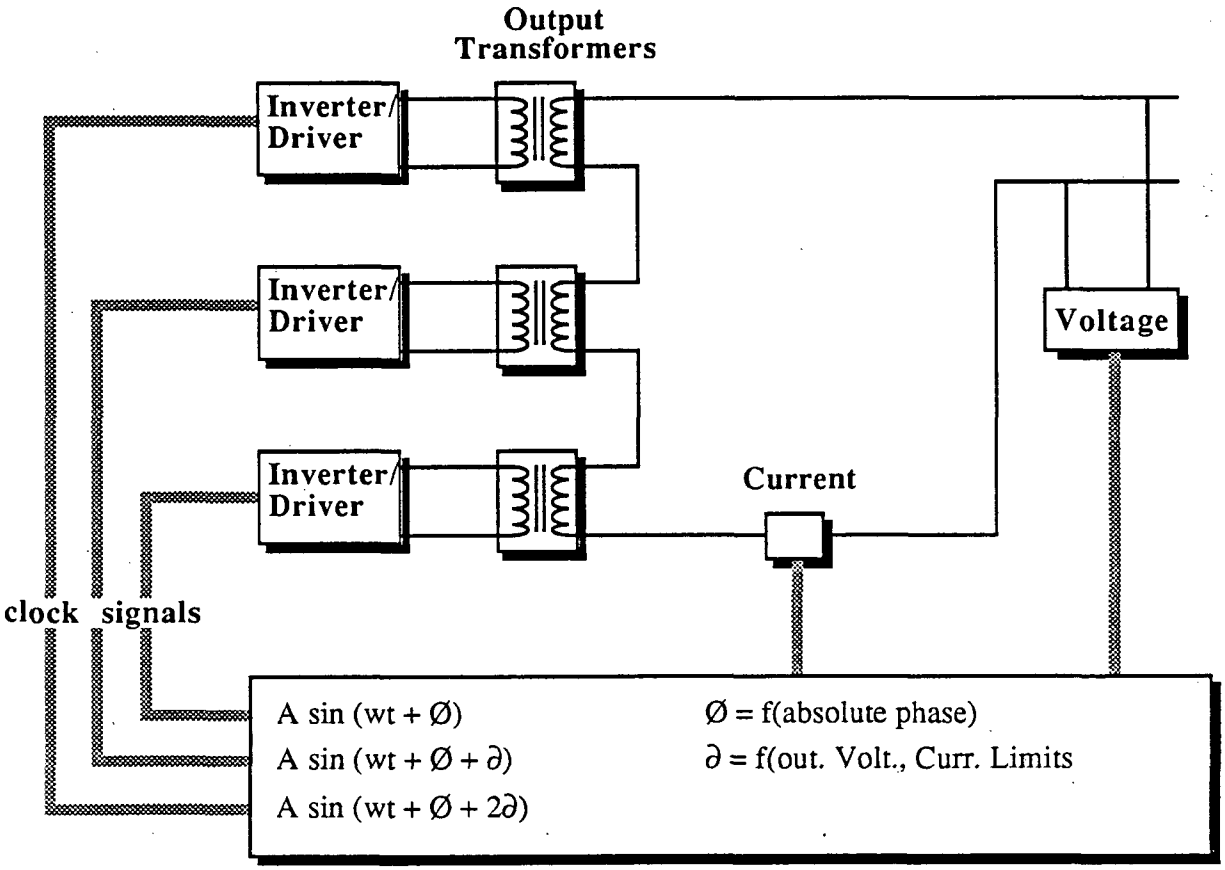

Figure 2-4. Basic Phasor Regulation Approach.

The pure load-interface modules process the 20-kHz transmission bus power to create the required user power forms. In all cases, the process is basically a traditional AC rectification type. Output amplitude control is accomplished by pulse-population or phase-delay control of individual 20-kHz, half-sine pulses. The combination of amplitude control and individual pulse steering allow for the creation of a wide range of lower-frequency AC outputs. Figures 2-5 and 2-6 show typical (simplified) receiver configurations for DC and low-frequency AC outputs.

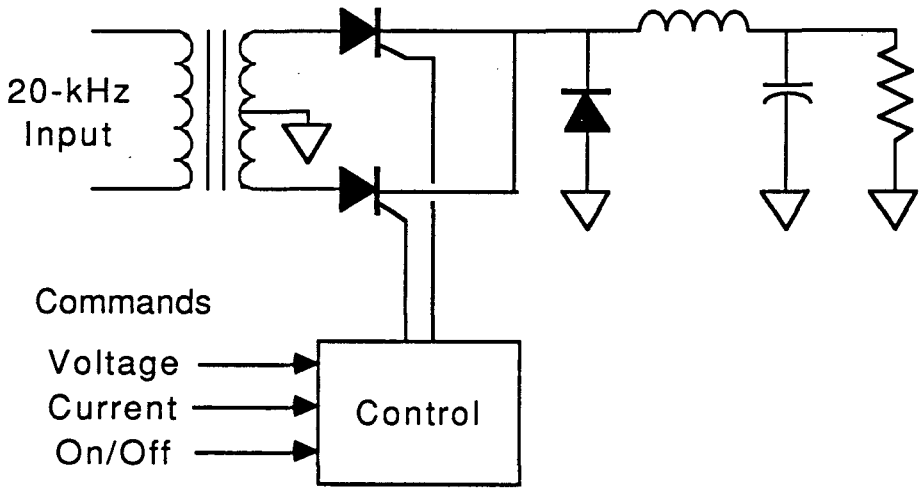

Figure 2-5. Typical DC Receiver output circuitry

The fifth receiver module takes advantage of the the inherent bilateral nature of this class of hardware to be both source and load interface. In the load interface mode, its thyristors are switched so that it looks just like the above-described DC receiver. In the source mode, its switches operate to make it an inverter.

Finally, there are many classes of loads that can use the 20-kHz bus power directly. Simple transformer coupling can be used to supply lighting (both fluorescent and incandescent), resistance heaters, simple induction heaters, etc.

2.2 Control Circuit Development Program (NAS 3-23878)

Bidirectional Power Converter Control Electronics

This program was aimed at developing a family of control circuit designs for resonant technology, power processing hardware; which were appropriate to control the SCR- driven,

power-switching stages and series resonant networks of "Mapham"-derived inverter/converter configurations (Reference 1).

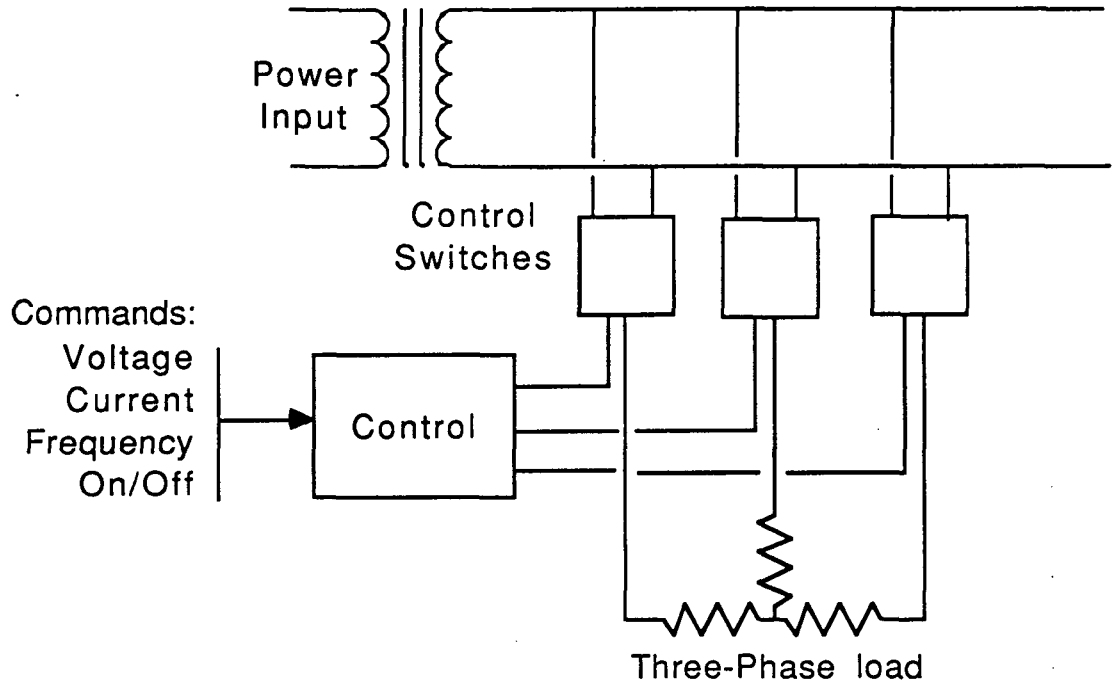

Figure 2-6. Three-phase, low-frequency AC output circuitry

In general,the primary tasks included the following:

- Analyze the basic set of functions required to control a multi-phase bidirectional resonant power system.
- Create a set of basic designs to implement those functions.
- Build and test the basic designs
- Integrate and test the control hardware into high-power breadboard/testbed systems.

Application specific power processor requirements addressed both source and load interfaces and included regulating drivers/inverters/frequency changers to provide high-frequency (20 kHz) AC from DC or low-frequency AC; and bidirectional interfaces from 20-kHz AC to DC or low-frequency AC loads and users. The main functions were broken into two sections and

defined as follows:

2.2.1 General

- Housekeeping
- Overload Protection

2.2.2 Application Specific

- Case 1: On-board battery charging from the high-frequency bus.
- Case 2: Auxiliary ground power energizing the high-frequency bus.
- Case 3: Variable-speed motor/generator starting/running/generation to and from the high-frequency bus.

The control circuit designs developed by this program are the basic control modules required for the breadboard hardware functions. See Figure 2-7 for an example of the control modules used in an inverter configuration. Those designs were carried forward to be the controls for the breadboard contract power stages. Reference 2 documents the details of the control development. As testing and troubleshooting of the breadboard hardware progressed, some changes were required, and the schematics and hardware drawings presented in this report are the updated ones.

2.3 Overall Breadboard Contract Tasks

2.3.1 Design and Development

The breadboard hardware was designed to simulate a typical Space Station power system on a much smaller power level. The set of receiver modules represented the major classifications of load interfaces that might be required on a real station. DC outputs, at a wide range of values; three-phase and single-phase AC outputs for motor operation and control; and a bidirectional module, to demonstrate a typical energy storage interface.

The major elements of the hardware design and development were accomplished prior to the start of this contract. Basic power component circuit designs were previously accomplished on Independent Research and Development programs at General Dynamics and the control circuit designs were performed on the Bidirectional Power Converter Control Electronics program described in Section 2.2. This program mainly addressed the

system design details not previously examined. System interactions evaluated during the debugging and testing phases of the program resulted in some redesigns of the previously-developed hardware, and those redesigns were included in the tasks accomplished on this development.

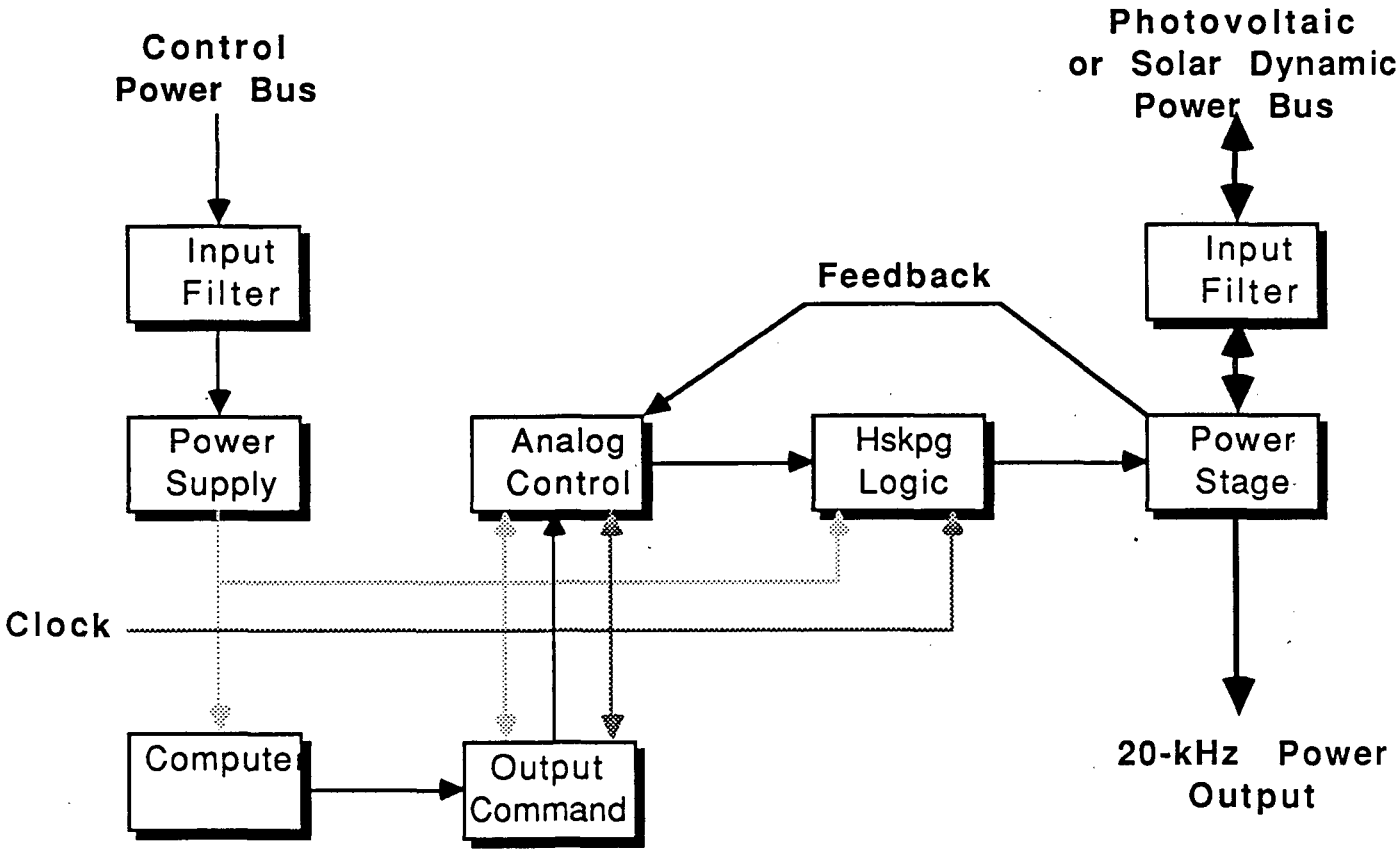

Figure 2-7. Basic Inverter Control

2.3.2 Fabrication

The fabrication task was to procure the appropriate hardware, and to actually construct the breadboard hardware to simulate a major portion of a typical Space Station configuration. It was constructed in two modular groups (drivers and receivers), interconnected by a pair of redundant 50 meter power busses.

Because of the developmental nature of the hardware, construction and fabrication tasks were accomplished by avionics technicians working under the direct supervision of the

design engineers.

2.3.3 Test

The test program actually operated on two levels.

First, the constructed hardware was debugged and tested as modules and subassemblies, and then assembled into a complete system for additional debugging and verification testing.

Once proper operation was demonstrated, an acceptance test was performed to verify that the hardware met all its requirements and was ready for delivery.

2.3.4 Delivery

The delivery task included the transfer of the hardware to NASA, Marshall Space Flight Center in Huntsville, Alabama, and assistance to NASA to set up and operate the equipment in their facility at Marshall Space Flight Center. The official acceptance test was performed after the installation in the NASA facility was complete.

3.0 Hardware Design and Development

3.1 Requirements Specification

3.1.1 Work Statement

The requirements for breadboard operation are all contained in the contract work statement. Rather than repeat them in this text, a copy of the appropriate sections of the actual work statement is included as Appendix A of this report. Appendix B is a digest of the the hardware detailed requirements.

3.1.2 Requirements Changes

As the program evolved and the Space Station became better defined, some of the requirements for this breadboard hardware changed. In addition, some hardware requirements were relaxed to avoid the unnecessary expenditure of resources to exactly meet some work statement detail, once the basic principle of operation had been defined and fully demonstrated. The last two columns of the tables of Appendix B show the subsequent deviations from the original requirements.

3.2 Overall System Design

Overall system design was based on earlier studies and breadboard programs (References 3,4,5,6) performed by NASA and General Dynamics. The primary goal was to provide a reduced size demonstration and engineering development breadboard of a high-frequency (20 kHz) Power Management and Distribution system.

That system (see Figure 3-1) included a set of regulating inverter modules to demonstrate multiple source modularity, paralleling, and load sharing; and a matching set of Remote Power Controllers for fault management and switching.

Two fifty-meter power distribution busses were included to evaluate transmission line parameters and phenomena.

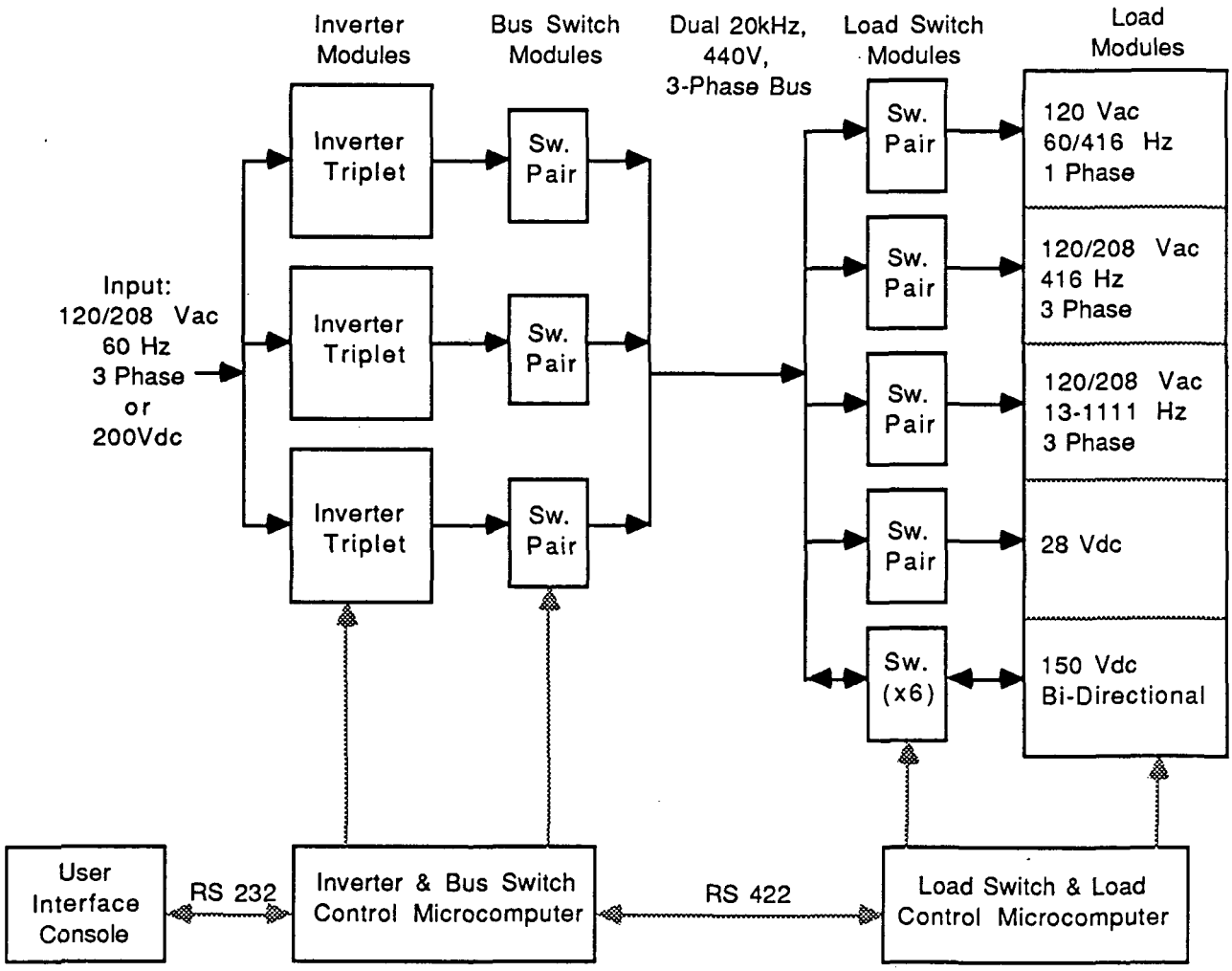

Figure 3-1. Breadboard Block Diagram

A representative set of receiver (load interface) modules was also included to evaluate the system impacts of the likely station loads and to determine any special design considerations or constraints for the users. One single-phase and two three-phase, variable frequency, variable-voltage AC receivers were constructed to evaluate low-frequency AC output interfaces. A variable-voltage (nominally 28 V) DC module was constructed to evaluate DC output interfaces. The bidirectional receiver module was required to evaluate the energy storage interfaces and to provide for additional paralleling data when the sources are widely separated and of different character. Remote Power Controllers were also included at the receiver module inputs to provide for fault isolation.

Full computer control, simulating Space Station-type operation, was also a major requirement. Embedded processors were included in both driver and receiver assemblies. Even though the exact type which will be selected for the Space Station flight application is not currently known, these embedded processors were used to define, implement, and test the basic hardware interfaces, control algorithms, and software instructions applicable to this class of hardware. An operator interface was provided using a Macintosh™ computer, which communicated with the embedded computers through a serial data bus, thereby simulating the Space Station Electrical Power System computer-to-embedded computer link for overall command and data functions.

3.3 Predesign

The predesign phase for this program was not the usual evaluation of circuit options in response to requirements of a new design and development task. Since the primary control circuits were previously developed on the Bidirectional Power Converter Control Electronics contract and the basic power circuit design came from previous Independent Research and Development work, this part of the task was reduced to evaluating those designs for appropriateness to the requirements of this deliverable breadboard hardware. The predesign phase also highlighted any areas where design changes might be required.

3.4 Control Design

3.4.1 Logic and Interfaces

Digital control functions and interfaces provide for all the basic control of power switch operation including housekeeping, mode control, frequency synthesis, and clocking and timing. They are consistent with the operation and design developed in the Bidirectional Power Converter Control Electronics contract. See Reference 2 for a complete discussion of the design and operation of these circuit modules. Reference 7 is a more general discussion of the control of resonant power processors. Appendix C is a set of hardware schematics, which will show the actual circuits involved.

3.4.2 Analog Control

The output voltage regulation and limiting functions are the only analog control circuits in this hardware. The regulators function as first order closed-loop feedback controllers. With their references provided by computer Digital-to-Analog inputs, they provide all the flexibility of computer control, and the frequency response and stability of the first order

analog system.

These basic designs were also developed in the Bidirectional Power Converter Control Electronics contract. See References 2 and 7 for a complete discussion of the design and operation of these circuit modules. Appendix C also contains these schematics.

3.4.3 Computers

See Figure 3-2 for a conceptual drawing of the computer system.

3.4.3.1 Computer System Control Primary Requirements

- Embedded Microprocessor Control
- Interfaces: RS-232, RS-422 serial data busses
- Monitor Analog Data
- Accept Data Bus Commands
- Serial Data Bus Input and Output
- Interface with Breadboard Facility System at Marshall Space Flight Center
- Self Check

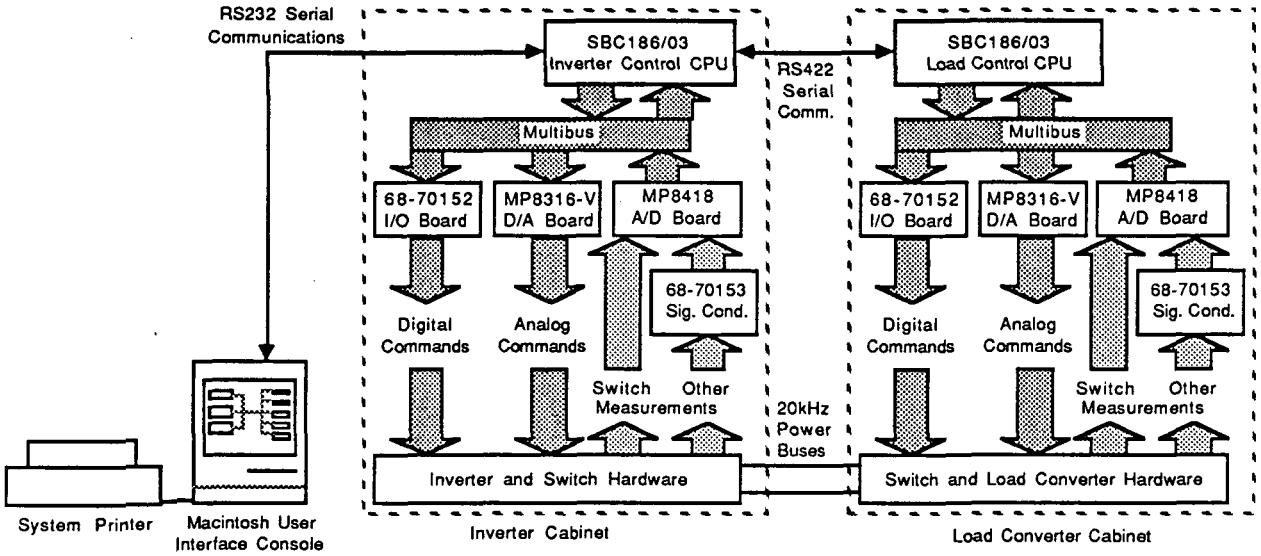

Figure 3-2. Computer System Block Diagram

3.4.3.2 System Control Design Features

- Macintosh™ supervisory controller and operator interface
- Embedded 8086 type processors in source and load cabinets
- Programmed in Microsoft™ Basic and Intel PL/M™

• Controls all system functions and levels

3.4.3.3 Terminal/Supervisor - This hardware is a Macintosh™ computer providing an easy-to-learn, user-friendly operator interface with a serial data bus output, simulating the Electrical Power System-to-embedded computer interface on the Space Station. Full use of the Macintosh operating environment is provided with pull-down menus, graphics command and monitoring screens and windows, and full mouse control.

The system is controlled from three windows on the Macintosh. Any module can be enabled or disabled from the On/Off Screen (Figure 3-3). The parameters of each module, such as voltage, current, and frequency are set from the Set Values Screen (Figure 3-4). The data monitored on the breadboard is reported on the Measurements Screen (Figure 3-5).

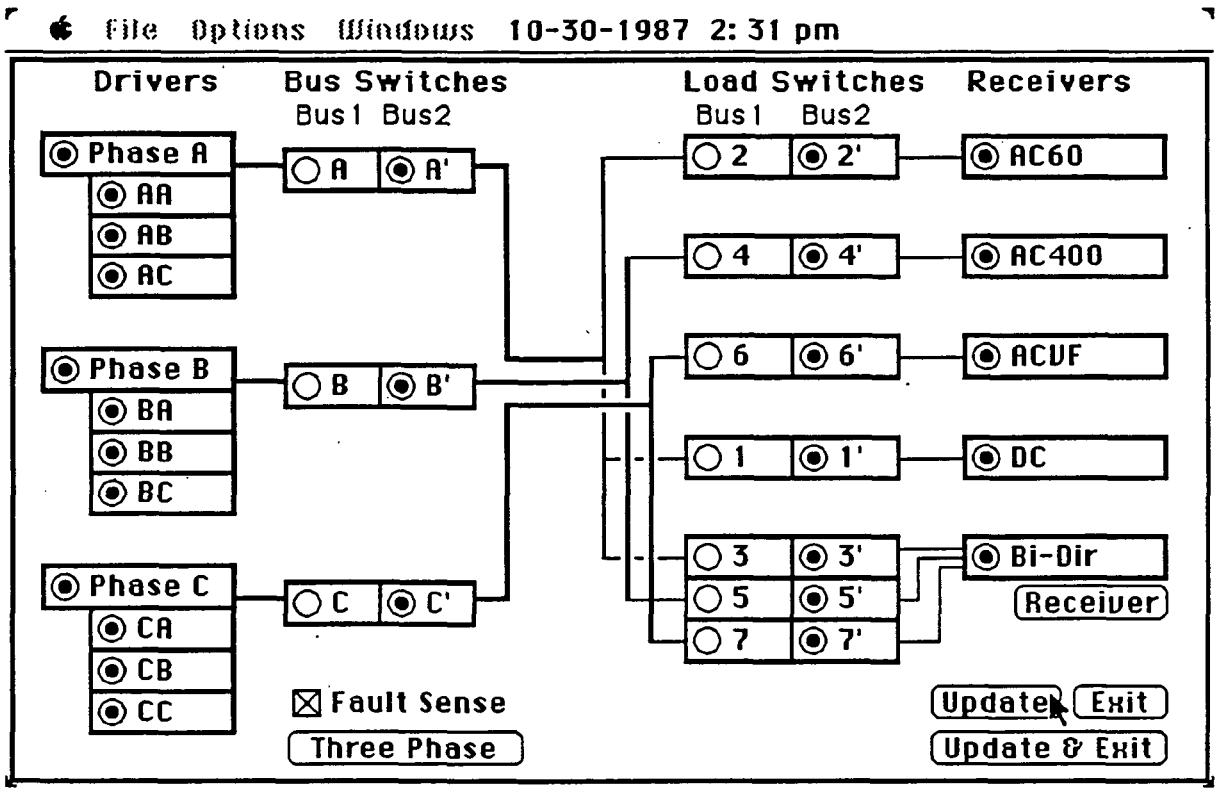

Figure 3-3. The system modules are enabled from the On/Off Screen.

Operation of the hardware is fully documented in the Operation and Service Manual provided as one of the deliverables with this equipment. The reader is referred to that source for additional detailed data.

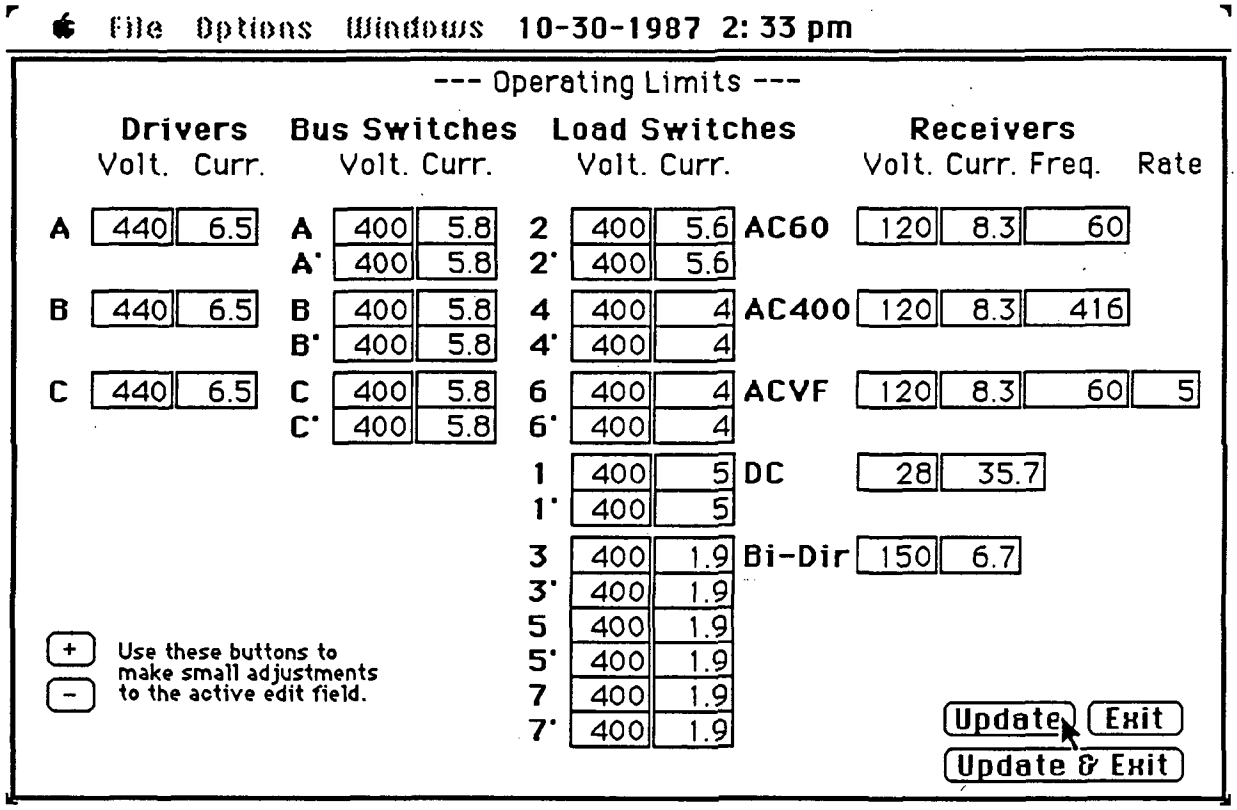

Figure 3-4. The system parameters are set from the Set Values Screen.

3.4.3.4 Embedded Processors - The embedded computers are Intel SBC 186/03 single board computers, packaged in a MultiBus™ card cage. They interface with four other MultiBus™ compatible cards, which are the primary interfaces with the power processing hardware. A Burr-Brown™ Digital-to-Analog converter board provides the set of 16 analog references to be used by the control loops. A Burr-Brown™ analog-to-digital converter board provides 32 channels of analog data monitoring for the basic instrumentation functions. The set also includes two interface boards. An RMS-to-DC converter board is used to condition the AC input data to a DC form readable by the Analog-to-Digital board. A discrete interface board provides latching and adjusts the 5-volt computer logic signals to the 15-volt levels required by the CMOS system logic hardware, for on-off discretes, mode control

commands, etc.

Operation of this hardware is also fully documented in the Operation and Service Manual provided as one of the deliverables with this equipment, and the reader is referred to that source for additional detailed data.

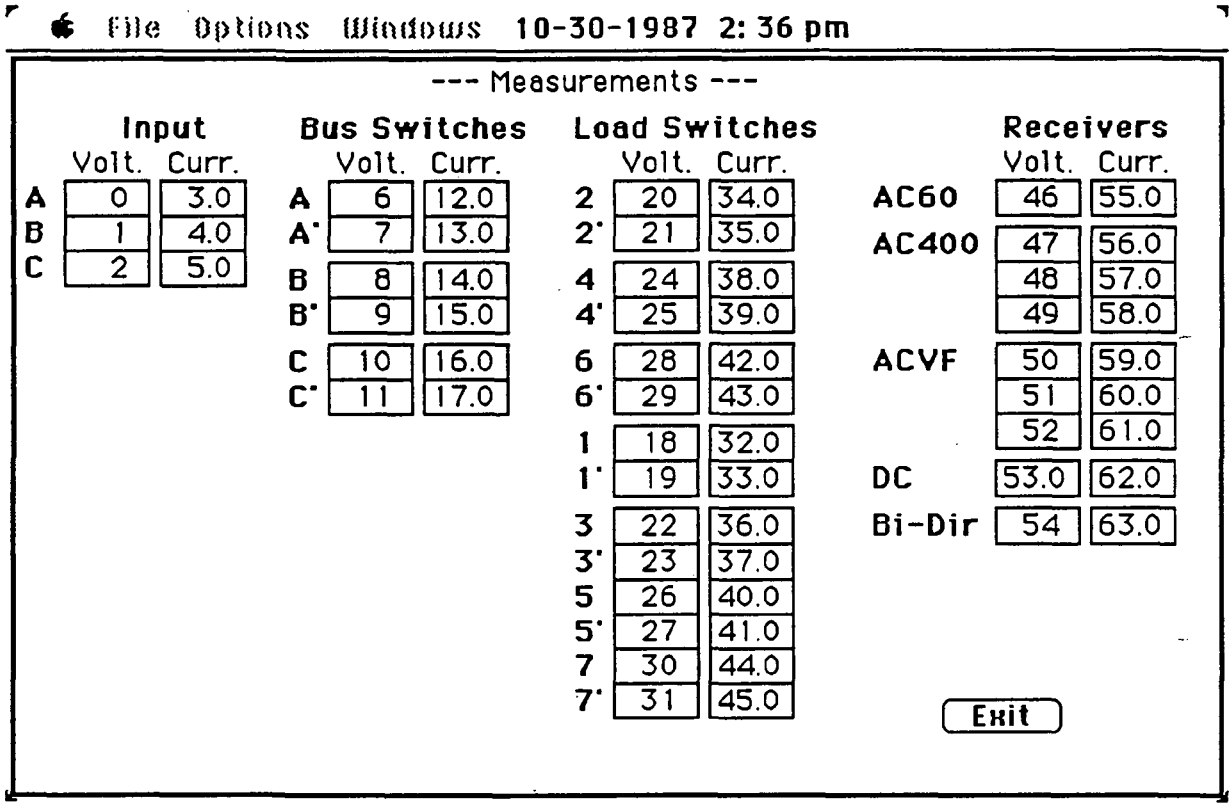

Figure 3-5. System data is displayed on the Measurement Screen.

3.4.4 Software

3.4.4.1 Terminal/Supervisor - This is software which runs the operator interface, issues the overall system commands, scales and displays system operating data, and monitors system operational status. It runs on the Macintosh operator interface computer and is written in Microsoft™ Basic so that it can be easily understood and modified by the user, when he elects to change some aspect of the breadboard operation. Figure 3-6 presents an overview of the software design.

This software is fully documented (including flow charts and listings) in the Operation and Service Manual provided as one of the deliverables with this equipment, and the reader is referred to that source for additional detailed data about this software.

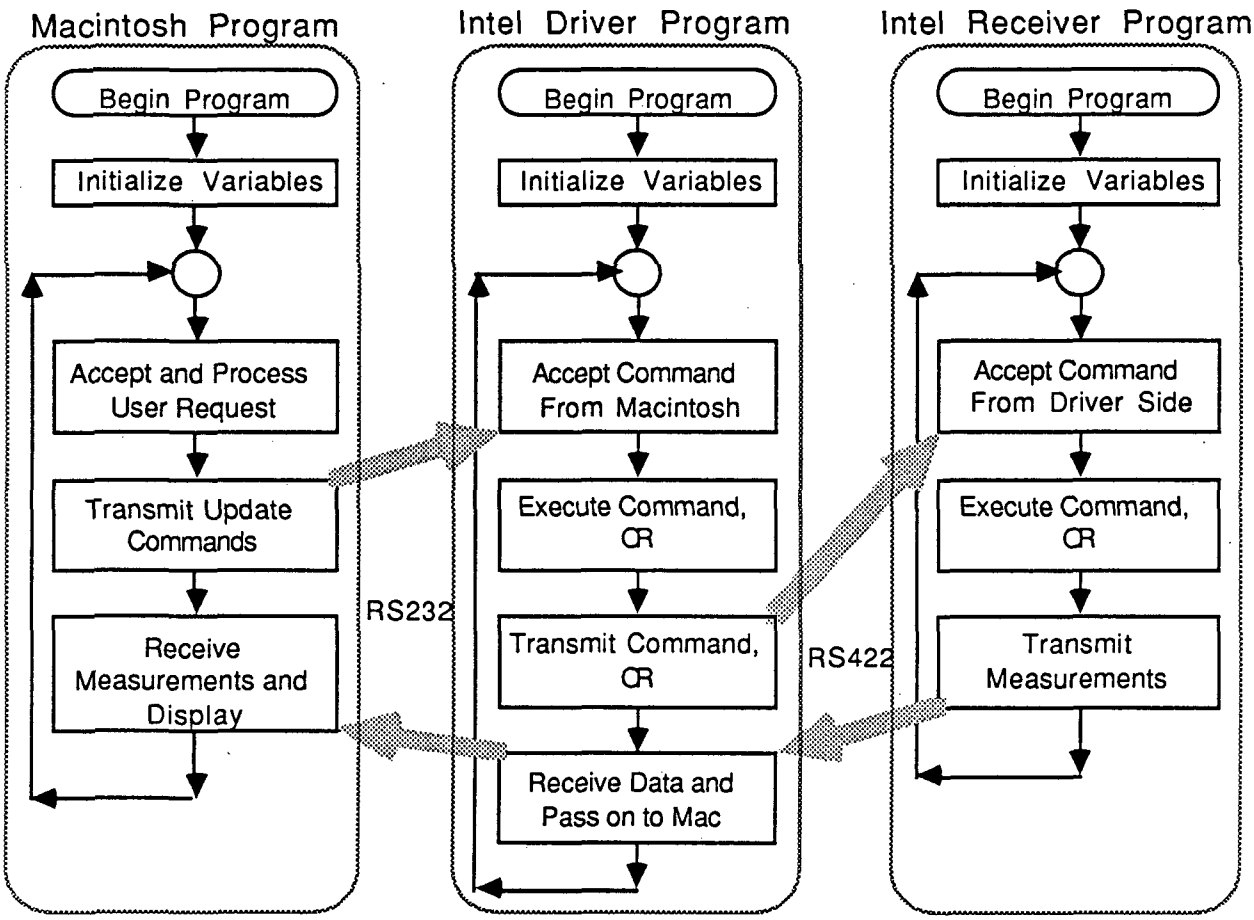

Figure 3-6. Software System Flow Diagram

3.4.4.2 Embedded Processors - Since the embedded computers are Intel™ 8086 type processors, they were programmed in PL/M, a high level Pascal-like language specifically written for this computer version and its development system. As above, this software is fully documented (including flow charts and listings) in the Operation and Service Manual provided as on of the deliverables with this equipment. The reader is referred to that source for additional detailed data about this software.

3.5 Power Module/Circuit Design

Since the basic power circuit designs were created on Independent Research and Development programs and earlier contracts, the details of their design processes will not be recounted here. Additional information may be found in References 5 and 6. The following paragraphs will cover the primary detailed requirements that the major items of breadboard hardware meet, and each of the assembly's important design features.

3.5.1 Resonant Driver (Inverter)

See Figure 3-7 for a conceptual drawing of the inverter power stage.

3.5.1.1 Inverter Primary Requirements

- Input Voltage: 120/208 Vac RMS three phase, or 200 VDC
- Output Voltage: 440 Vac RMS, ±5.0% single phase or three phase
- Output Power: 5 kW, total, maximum
- Output Frequency: 20 kHz ±1%
- Load Variation: Operate with any combination of loads removed

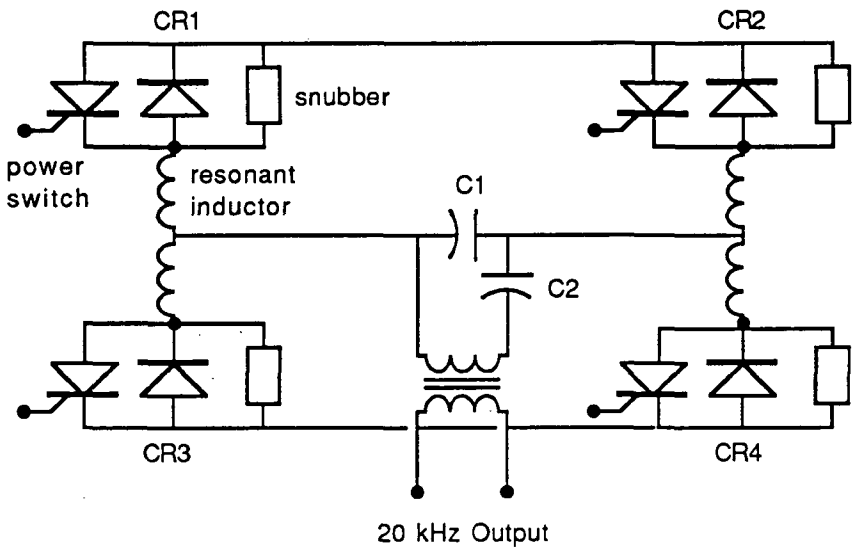

Figure 3-7. Driver/Inverter Power Stage

3.5.1.2 Inverter Design Features

- Utilizes resonant conversion (in basic "Mapham" configuration)
- "Utility" characteristics

- Phasor regulation for AC output control
- Multiple modules, operating in parallel
- Utilizes control designs from Bidirectional Power Converter Control Electronics Contract, NAS 3-23878

3.5.2 Source Switches (Remote Power Controller)

See Figure 3-8 for a conceptual drawing of the switch elements.

3.5.2.1 Switch Matrix (Remote Power Controller) Primary Requirements

- Turn on and turn off with computer/controller command, response less than 100 msec.
- Automatic turn off based on voltage/current threshold
- Switched Voltage = 762 VAC,RMS ±5%
- Switched Current = 5 amp, AC, RMS max. (real)
- Response time (TBD) = 50 μsec, max.

3.5.2.2 Remote Power Controller Design Features

- Antiparallel SCRs for series switch element
- Thresholds fully computer controlled
- Source and load switches the same

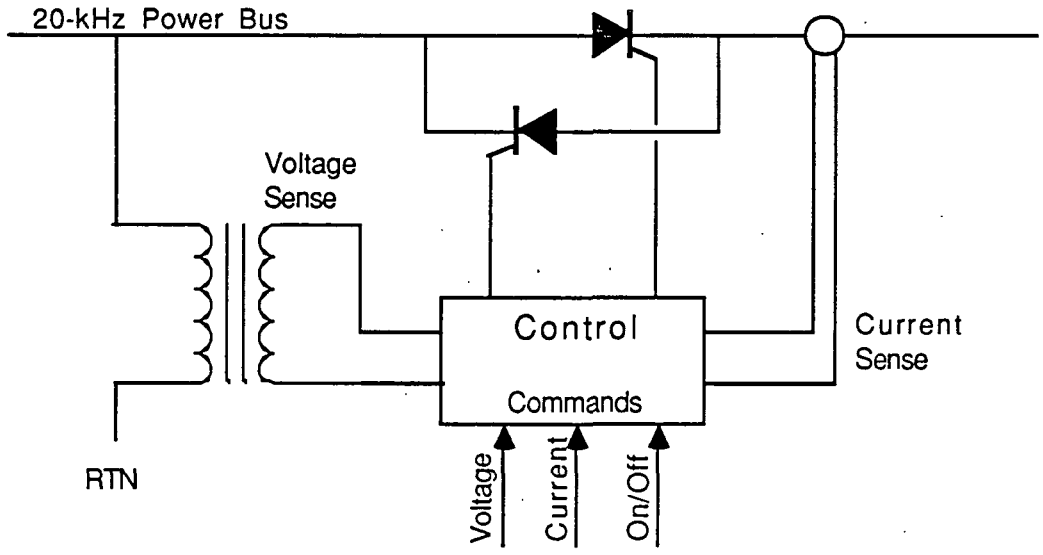

Figure 3-8. Remote Power Controller Conceptual Schematic

3.5.3 Transmission line

The power bus design for this program consisted of three coaxial cables per bus. The three coaxial cables are constructed of litz-wire center conductors and braided-shield outer conductors. The three coax cables are twisted and encased in a shield. Each coaxial cable is used for one phase. As such, the busses can be used in either a three-phase or single-phase mode. See Figure 3-9 for a cross section of the bus configuration used in the evaluation testing.

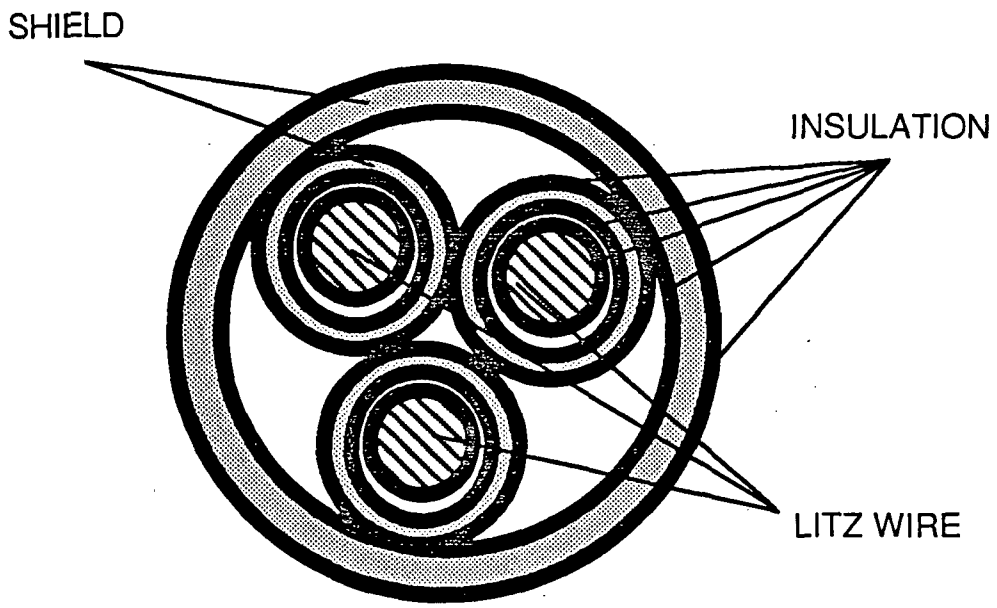

Figure 3-9. Transmission Line Design Cross Section

3.5.3.1 Power Bus System Primary Requirements

- Three phase, four wire; or Single phase, six wire
- Length = 50 meters, minimum
- Voltage = 440 VAC, RMS,±5%
- Current = 5 amp, RMS (normal load)
  10 amp, RMS (fault operation)
- Allowable Losses = 0.5% of load (normal load)
  2.0% of load (fault operation)
- Terminations (TBD) = standard MIL- connectors
- Capacitance (TBD) = 0.30 nfarad/meter (twisted pair design)
- Inductance (TBD) = 0.35 μhenry/meter (twisted pair design)

3.5.3.2 Power Bus Design Features (twisted pair design)

- Shielded, twisted pair configuration
- Constructed of Litz Wire

3.5.4 Receiver Switches (Remote Power Controller)

See Figure 3-8 .

3.5.4.1 Switch Matrix (Remote Power Controller) Primary Requirements

- Turn on and turn off with computer/controller command, response less than 100 msec.
- Automatic turn off based on voltage/current threshold
- Switched Voltage = 440 VAC,RMS ±5%
- Switched Current = 5.0 amp, AC, RMS max.
- Response time (TBD) = 50 μsec, max.

3.5.4.2 Remote Power Controller Design Features

- Antiparallel SCRs for series switch element
- Thresholds fully computer controlled
- Source and load switches the same

3.5.5 400-Hz, Three-Phase AC Receiver

See Figure 3-10 for a conceptual drawing of the output connections.

3.5.5.1 400-Hz, Three-Phase AC Receiver Module Primary Requirements

- Input Voltage = 440 VAC, RMS ±5%
- Input frequency = 20.0 kHz
- Output Voltage = 120/208 VAC, RMS ±5.0%, three phase
- Output Frequency = 400 Hz, ±5.3%
- Output Power = 1.0 kW

3.5.5.2 400-Hz, Three-Phase AC Receiver Module Design Features

- Basic six-step design
- Input power factor control
- Output is computer controlled

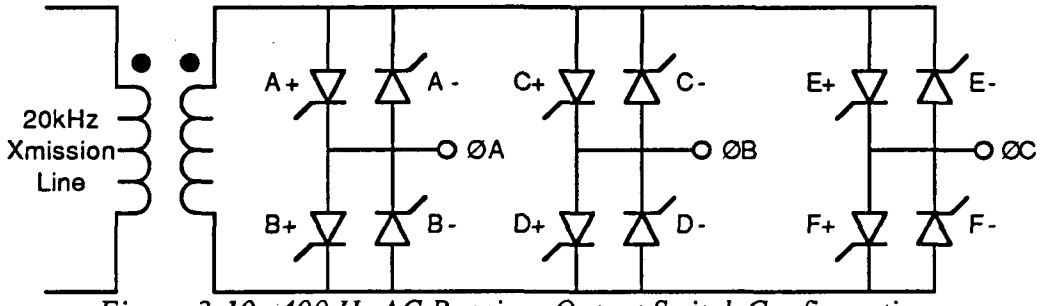

Figure 3-10. 400 Hz AC Receiver Output Switch Configuration

3.5.6 Single-Phase AC Receiver

See Figure 3-11 for a conceptual drawing of the output connections.

3.5.6.1 Single-Phase AC Receiver Module Primary Requirements

- Input Voltage = 440 VAC, RMS ±5%
- Input frequency = 20.0 kHz
- Output Voltage = 120 VAC, RMS ±5.0%, single phase
- Output Frequency = 60 Hz, ±1.0% or 400 Hz ±5.3%
- Output Power = 500 W

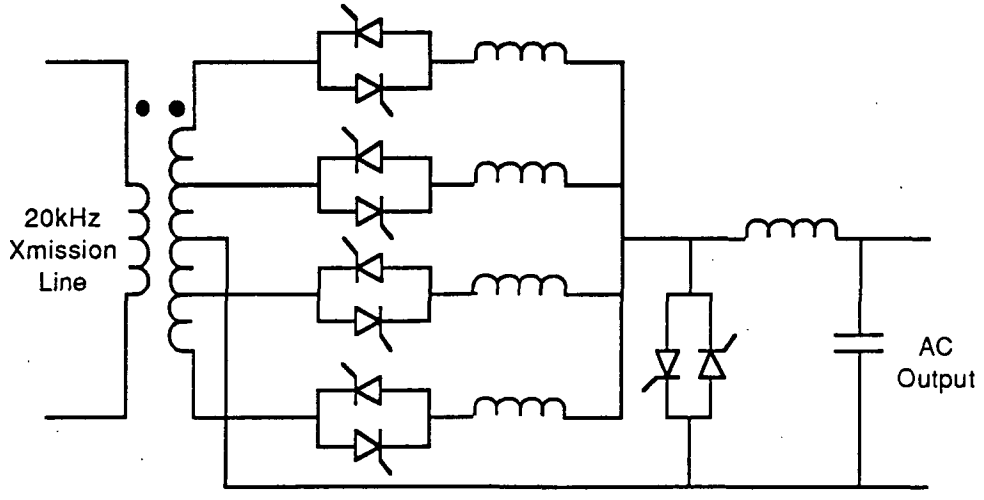

Figure 3-11. Single Phase AC Receiver Output Switch Configuration

3.5.6.2 Single-Phase AC Receiver Module Design Features

- Basic six-step design
- Input power factor control
- Output is computer controlled

Table 1. Any of these AC receiver frequencies (in Hz) may be selected with ±1% accuracy.

13	28	43	58	73	88	111	148	222	444
14	29	44	59	74	90	113	151	229	476
15	30	45	60	75	91	114	155	238	512
16	31	46	61	76	92	117	158	246	555
17	32	47	62	77	93	119	162	256	606
18	33	48	63	78	95	121	166	266	666
19	34	49	64	79	96	123	170	277	740
20	35	50	65	80	98	125	175	289	833
21	36	51	66	81	99	128	180	303	952
22	37	52	67	82	101	130	185	317	1111
23	38	53	68	83	102	133	190	333	
24	39	54	69	84	104	136	196	350	
25	40	55	70	85	105	138	202	370	
26	41	56	71	86	107	141	208	392	
27	42	57	72	87	109	144	215	416	

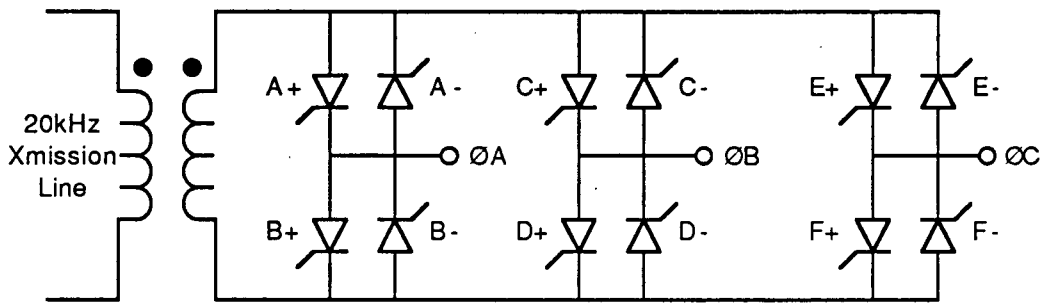

Figure 3-12. Variable Frequency AC Receiver Output Switch Configuration

3.5.7 Variable-Frequency, Variable-Voltage AC Receiver

See Figure 3-12 for a conceptual drawing of the output connections.

3.5.7.1 Variable-Voltage, Variable-Frequency, AC Receiver Module Primary Requirements

- Input Voltage = 440 VAC, RMS ±5%
- Input frequency = 20.0 kHz
- Output Voltage = 120/208 VAC, RMS ±5.0%, three phase
- Output Frequency = 13 Hz to 1.111 kHz in discrete frequencies as listed in Table 1
- Output Power = 1.0 kW

3.5.7.2 Variable Voltage, Variable Frequency AC Receiver Module Design Features

- Basic six-step design
- Input power factor control
- Output is computer controlled

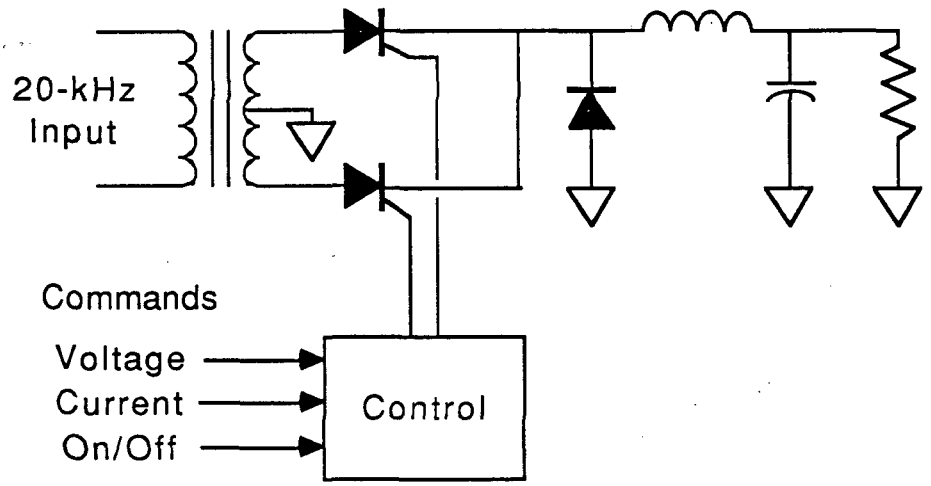

Figure 3-13. DC Receiver Power Output

3.5.8 DC Receiver

See Figure 3-13 for a conceptual drawing of the power output components.

3.5.8.1 Variable-Voltage DC Receiver Module Primary Requirements

- Input Voltage = 440 VAC,RMS ±5%

- Input frequency = 20.0 kHz
- Output Voltage = 28 VDC ±1 VDC
- Output Power = 1.0 kW

3.5.8.2 Variable Voltage DC Receiver Module Design Features

- Basic transformer/rectifier design
- Input power factor control
- Output is computer controlled

3.5.9 Bidirectional Receiver

See Figure 3-14 to verify the similarity to the inverter design. The main difference in the power handling stage is that the "flyback" diodes are replaced by SCRs.

3.5.9.1 Bidirectional DC Receiver Module Primary Requirements

- Input/Output Voltage = 440 VAC,RMS ±5%
- Input/Output frequency = 20.0 kHz ±1%
- Output/Input Voltage = 150 VDC
- Output Power = 1.0 kW

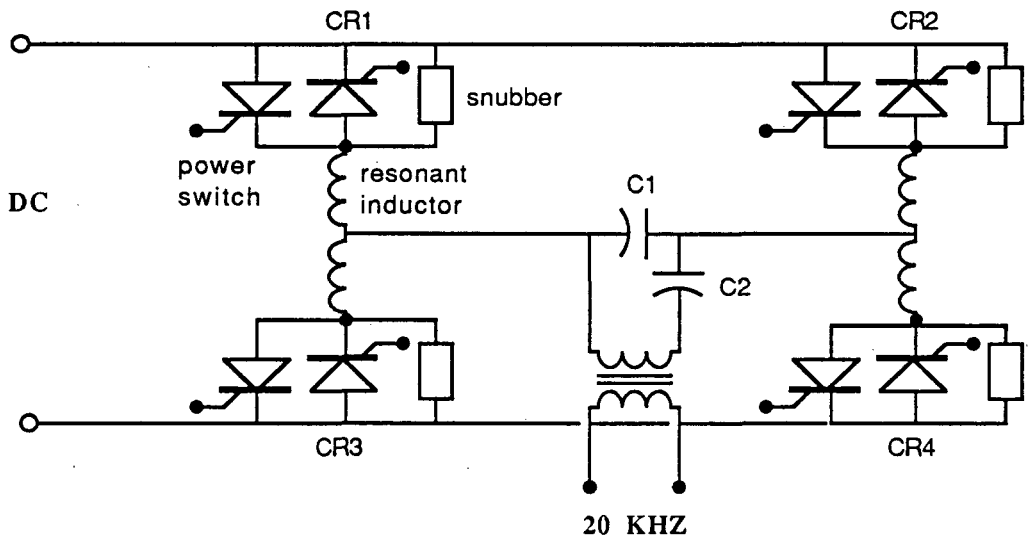

Figure 3-14. The Bidirectional Receiver power stage is similar to the Inverter. Six of these stages make up the Bidirectional Receiver.

3.5.9.2 Bidirectional DC Receiver Module Design Features

- Basic inverter/bridge design
- Phasor regulation for AC output control
- Inductor-capacitor output/input filter
- Input power factor control
- Output is computer controlled

3.6 Measurements and Instrumentation

3.6.1 Computer Measurements

All DC measurements are appropriately isolated and scaled to be compatible with the 0 to 10 volt range of the Burr-Brown standard bus analog-to-digital converter card. AC measurements are similarly isolated and scaled, but they are connected to the standard bus RMS-to-DC Converter card, where they are converted to scaled DC outputs, readable by the above Analog-to-Digital converter board.

High voltage AC measurements are taken through step-down transformers, and AC currents are measured through current transformers, designed specifically for the 20-kHz system frequency. These outputs are scaled and isolated with instrumentation amplifiers where required, and applied to the RMS-to-DC Converter board.

The high-voltage DC measurements are reduced to appropriate signal levels through a high-impedance resistive divider network, and the DC currents are measured from high-frequency, coaxial current shunts. Both are fed directly to the RMS-to-DC Converter board.

The computer measurements are obtained from the outputs of the analog-to-digital board which converts the 0 to 10 volt, DC signals to digital values from 0 to 4095. The digital number are then read by the computer and multiplied and scaled by the appropriate calibration factors. The final results are displayed in engineering units in the measurements window of the Macintosh interface.

3.6.2 Direct Measurements

Instrumentation points are provided throughout the assemblies for direct readouts of system performance. These signals are intended for connection of appropriate laboratory

instruments (input isolation, high voltage, high impedance, etc) and are not scaled, limited, or protected.

3.7 Mechanical Design

The mechanical design of the delivered hardware is consistent with the breadboard operations planned for its final end use. It was placed in roll-out drawers, mounted in standard laboratory "19 inch" racks, enclosed in EMI protective outer cabinets. Control and direct measurement accessibility is from the front of the cabinets, and all inputs and outputs are via standard connectors, mounted on the back panels. Hinged doors provide physical protection and EMI integrity.

3.7.1 Modular Layout

Modules and subassemblies were divided based on functional electrical and electronic blocks.

Control wire-wrap and circuit boards were divided into functional blocks developed in the Bidirectional Power Converter Control Electronics contract. Using this approach separates analog and logic functions into separate sub-assemblies. The logic functions are farther divided into functional blocks that can be common to several drivers or receivers, such as housekeeping, frequency synthesis, input/output, etc. This facilitates later development of a set of standard control blocks using semi-custom-IC or Programmable Array Logic implementations.

Power devices and associated resonant components were grouped into functional blocks to assess component sizes and layout requirements, so as to provide preliminary information to packaging studies which evaluated and sized expected flight designs.

The actual modular breakdowns and their combinations to construct higher order functions can be examined in the complete report of Reference 2.

3.7.2 Driver Cabinet

The driver (inverter) assembly was housed in a two-bay, six-foot, standard 19 inch rack size, EMI compatible enclosure. (See Figure 3-15.)

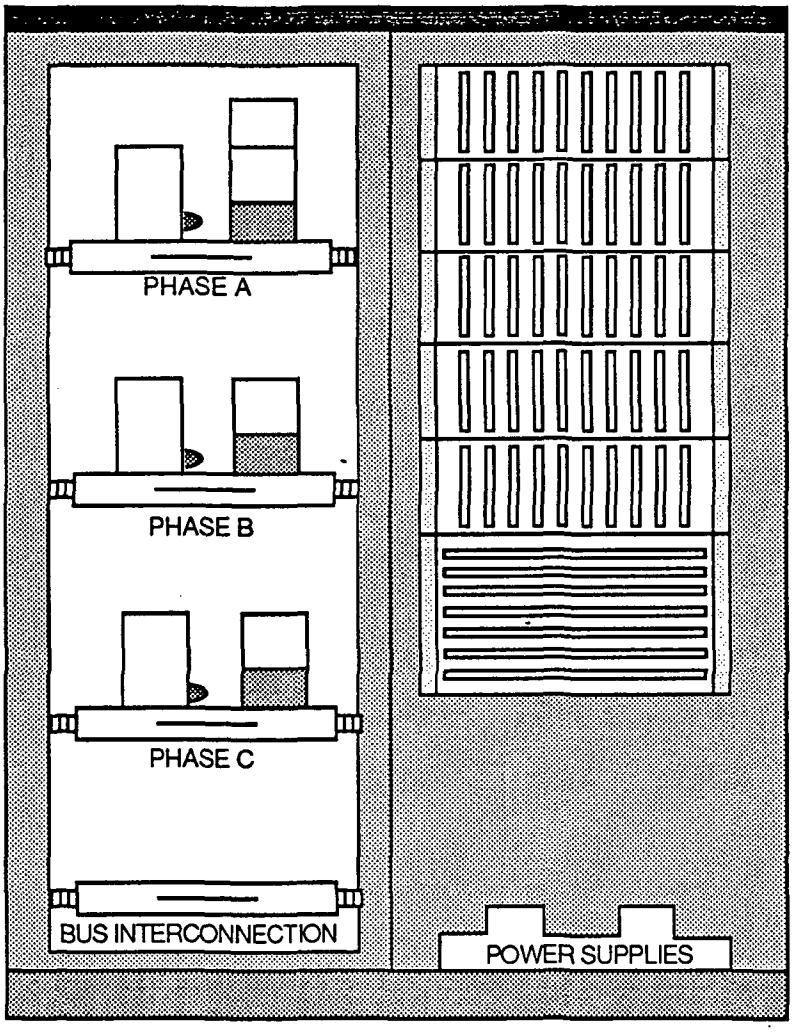

Figure 3-15. Driver Cabinet

One bay contains the high power equipment and logic circuits. The inverter power stages and resonant circuit components are arranged with a regulating set of three inverters and its dual output control Remote Power Controllers in each of three roll-out drawers. The output transformers are also mounted in the drawer.

The two transmission lines are connected to the output of the inverters and Remote Power Controllers with two interconnection panels located in the fourth drawer at the bottom of the cabinet. High-power, 20-kHz connections from individual inverters to their respective output transformers, from the interconnection panel to the output connectors at the back panel, and from the inverters and Remote Power Controllers to the interconnection panel of

the cabinet are Litz wire. This is to minimize skin-effect losses.

The other bay contains all the control circuitry and the embedded computer for the inverter assembly. The 8086-type embedded processor and its input and output boards are housed in their own "standard bus" card cage. The logic and control circuitry is assembled on wire-wrap and printed circuit cards, plugged into card cages and interconnected via conventional back-plane wiring and ribbon cables. Drive, feedback, and instrumentation signals are passed between cabinet sections through shielded, twisted-pair, cables and 37-pin connectors. All input and output interfaces are terminated with conventional connectors on the cabinet back panels.

3.7.3 Receiver Cabinet

The basic mechanical arrangement of the receiver assembly is the same as the inverters, and the same basic cabinet type is used. The power components are housed in one bay of a two bay set. As in the inverters, all the control circuitry, including the receiver assembly embedded processor, is housed in its own separate bay. (See Figure 3-11.)

3.7.4 Power Bus Systems

The breadboard uses a redundant set of two power busses. The 50-meter busses are described in detail in Section 3.5.3. Over the course of system integration and testing, both 50-meter and 100-meter busses were used.

3.7.5 Thermal Design

Thermal design was conventional for air-cooled, laboratory-type, rack mounted equipment, used in the normal air conditioned, 1-G, laboratory environment. Forced air cooling, using the ambient surrounding air, was chosen for all the cabinets. It was implemented by installing commercial, rack-mounted fans in the bottom of each cabinet, which blow air up through the cabinets and out vents in the cabinet tops.

An "outside-limit" type analysis was performed on the rack with the highest dissipation (inverter power rack) and a dual fan assembly, having an airflow of 300 CFM was selected. The same fan assembly was then used in all the racks, in the interest of commonality.

Cautionary Note: When operating the breadboard at full load, the drawers should be in their full "in" positions and the doors should be closed to assure adequate cooling for all the power components.

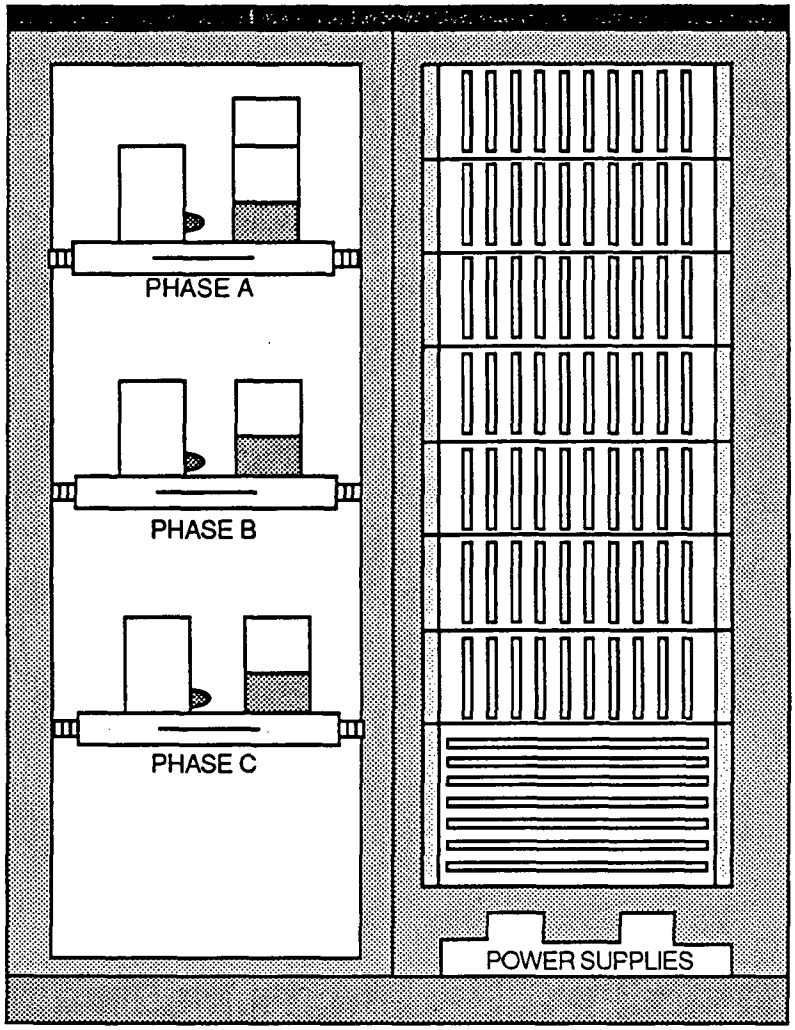

Figure 3-16. Receiver Cabinet

4.0 Fabrication

4.1 Electronic Piece Parts

All parts used in the construction of this equipment were commercial grade. Integrated circuits were primarily 4000-series CMOS and LS type TTL (at the computer interfaces) in plastic packages. Magnetic components were custom-designed (mostly with ferrite cores, wound with Litz wire), built to breadboard quality, and not potted. While resonant capacitors were selected to be low-loss types; special-purpose, high-frequency, high-power custom devices were not used.

4.2 Modules and Sub-assemblies

Wire-wrap circuit boards and power component assemblies were constructed by General Dynamics – Space Systems Division in our avionics assembly area, a special facility used for one-of-a-kind assemblies of this type. Printed circuit boards were manufactured and assembled to commercial standards by local subcontractors to reduce costs on higher quantity sub-assemblies.

4.3 Mechanical Assemblies

The majority of mechanical assembly items were commercial hardware, designed to be compatible with the cabinet/rack system selected. Standard catalog, forced-air heat sinks and power component mounting provisions were used. Standard card cages were selected for the control hardware rack. Small, special-purpose parts, such as mounting brackets or protective shields were constructed in our development machine shop.

4.4 Integrated Assembly

Integration and assembly into the final configuration was accomplished in the Space Power Systems laboratory, using research and development technicians, supervised by Space Power Group engineers.

4.5 Other Considerations

4.5.1 Laboratory Operations

All laboratory operations including part procurement, construction, and testing was controlled and supervised by Space Power Engineering personnel. Actual construction and test tasks were performed by Avionics engineering technicians and assemblers.

4.5.2 Quality Control

Quality standards for construction, inspection, and test were consistent with "good commercial practice". Conformance to these standards was monitored primarily by engineering, with the results observed by the Quality Department on a sample basis. No official monitoring or inspection by the Quality Control Department was required by the contract.

5.0 Testing and Discussion of Results

5.1 Test Plan

A formal, step-by-step test procedure was used for the operation and test of the breadboard hardware. A basic test plan, defining the data that was required for proper evaluation was written, and is included in this report as Appendix D.

5.2 Module and Sub-Assembly Testing

Since the hardware for this program is basically one-of-a-kind, no formal sub-assembly test sets were built, and initial verification of proper operation for the various system modules and sub-assemblies was performed on an informal basis, using standard laboratory test equipment, arranged in breadboard type test setups.

5.3 Integrated System Functional Testing

Once proper operation was established for the system elements, they were interconnected into a system configuration. Functional testing and integration proceeded in a sequential fashion.

5.3.1 Inverters

The inverters were powered and no-load operation was verified for each sub-unit. They were then operated into resistive loads, interconnected and paralleled for shared operation into resistive loads, and the power transmission line attached with the resistive loads moved to its end. When inverter operation was fully verified under these conditions, receiver modules were added to the system configuration. Finally, the Remote Power Controllers were added to the system and their operation verified.

During these tests, it became clear that the inverters did not properly share output loads when paralleled at light loads. Evaluation of the control function for the phasor regulator showed that under some conditions of load and inverter output voltage command, some inverters could sink current supplied by the others. The regulator control circuitry was redesigned, and the control boards changed to improve control of current sharing and to prevent inverters from sinking current.

5.3.2 Switches (Remote Power Controllers)

When the receivers were added to the system configuration, it was noted that the phase shifts caused by their filters, and the current distortions they reflected to the line caused improper operation of the system Remote Power Controllers, both at the driver and receiver ends of the power bus. Switch control designs referred the turn on to either line voltage or current, and there were times and load conditions which made neither the correct reference. Switch control designs were therefore changed to provide gate drive to the antiparallel SCRs whenever they are forward biased (making them independent of load phase and distortion) and the control boards were reworked to incorporate the new designs.

5.3.3 DC Receiver

The DC Receiver has unacceptably high third harmonic currents, and the low output impedance of the inverter-transmission line combination eliminated the interference as a problem for this case. Since this receiver does not meet the requirements of MIL-STD-461 (and other specs), more work must be done for a flight configuration.

5.3.4 Three-Phase AC Receivers (400 Hz and Variable-Frequency)

This type of AC three-phase receiver provides for a minimum of current modulation on the 20-kHz power bus, and therefore has a minimum impact on system operation. However, its regulator does have some of the same switching noise shown in the DC receiver.

In addition, the wide range of output frequencies required by this module's specification works well with a motor load, where the load is effectively its own output filter; but wide-band filtering for passive loads is not very practical. Therefore, while the controls for AC receivers may be designed to provide a wide range of output frequencies, the actual range of low frequency AC outputs into passive loads will be limited by the filter requirements.

5.3.5 Bidirectional Receiver

In the source (inverter) mode, this unit was operated from a master clock whose phase at the receiver matched the phase of the line voltage. Because the inverters had a different numbers of submodules (three) than the bidirectional (two), it was necessary to add phase control to the regulator control functions. Figures 5-1 through 5-6 show current sharing (for this class of hardware) as a function of the clock phase and commanded output

voltage.

5.4 Final Acceptance Test

The official, final acceptance test was performed at Marshall Space Flight Center, after the breadboard was shipped and installed, and returned to operating condition. The test was performed and proper operation was verified by Marshall Space Flight Center personnel, using a detailed Quality Verification Procedure written by General Dynamics.

5.4.1 Quality Verification (Acceptance Test) Procedure

The Quality Verification Procedure detailed the tests required to assure proper operation to the contract requirements of the AC power system breadboard. The tests included:

System Start Up / Steady State Test (ac input)
System Full Load Test — Three Phase, Single Bus (ac input)
DC Input Capability Test
System Full Load Test — Single Phase
Bidirectional (Driver Mode Operation) Verification
Three-Phase Bidirectional Load Sharing Verification
Single-Phase Bidirectional Load Sharing Verification
Fault Isolation Verification
Hard Fault Test
Power Factor Test

5.4.2. Test Results

Although the acceptance test was primarily functional in nature, some engineering data was recorded.The actual data is listed in the Performance Check Sheets of the QVP.

In addition to the acceptance test, several other tests were made during the program to provide information on the viability of 20kHz for use as a Space Station power distribution system. The important results ande conclusions derived from these tests are summarized below.

5.4.3 Summary and Discussion of Important Test Results

a. **Bidirectional Power Sharing** - A test was performed to determine the bidirectional receiver load sharing characteristics when driving the bus in parallel with the inverters. The test was performed with all three inverters, and all three bidirectional phases operating in the single phase mode, driving one single-phase bus. The bidirectional power output was characterized as a function of output voltage command and phase for a 1.1-kW and 3.0-kW resistive load, with the inverter and bidirectional input voltage held constant. The results of the test are shown in figures 5-1 through 5-6.

The graphs reveal some fundamental differences between the voltage and phase effects of modules operating in parallel. Namely, that the phase difference between the main 20-kHz reference and the module 20-kHz reference has a large effect on the power sharing between the modules. Alternatively, the voltage command of the modules has a large effect on the bus voltage. This suggests that a control scheme using both these parameters in the control loop will enable precise bus voltage control and individual inverter output power control. To raise or lower the bus voltage to account for varying demand, the controlling processor would alter the output voltage commands to the various modules. To control the power sharing between the "on line" modules, the processor would send phase lead/lag commands to the various modules.

b. **Power Transmission Bus Stability** - The MSFC testbed bus was a three phase, 50 meter twisted-pair type transmission line rated for 5 kVA which had the resistance, inductance, and capacitance values listed in table 5-1. The high series resistance and inductance values suggest that a twisted-pair type design is not optimum for the long power transmission cables of the Space Station. However, for short inter-module power cables, a simple twisted pair design may be sufficient.

Table 5-1 MSFC testbed and prototype Space Station transmission line impedances

	MSFC Testbed 5kVA	Induction General 25kVA
Parameter	50 meter 3Ø Bus	50 meter 1Ø Bus
Series Resistance	225 mΩ/phase	45 mΩ
Series Inductance	3.5 μH/phase	1.93 μH
Shunt Capacitance	.034 μF/phase	.069 μF
Capacitive kVA @ 440V	2.5 kVARs total	1.7 kVARs total

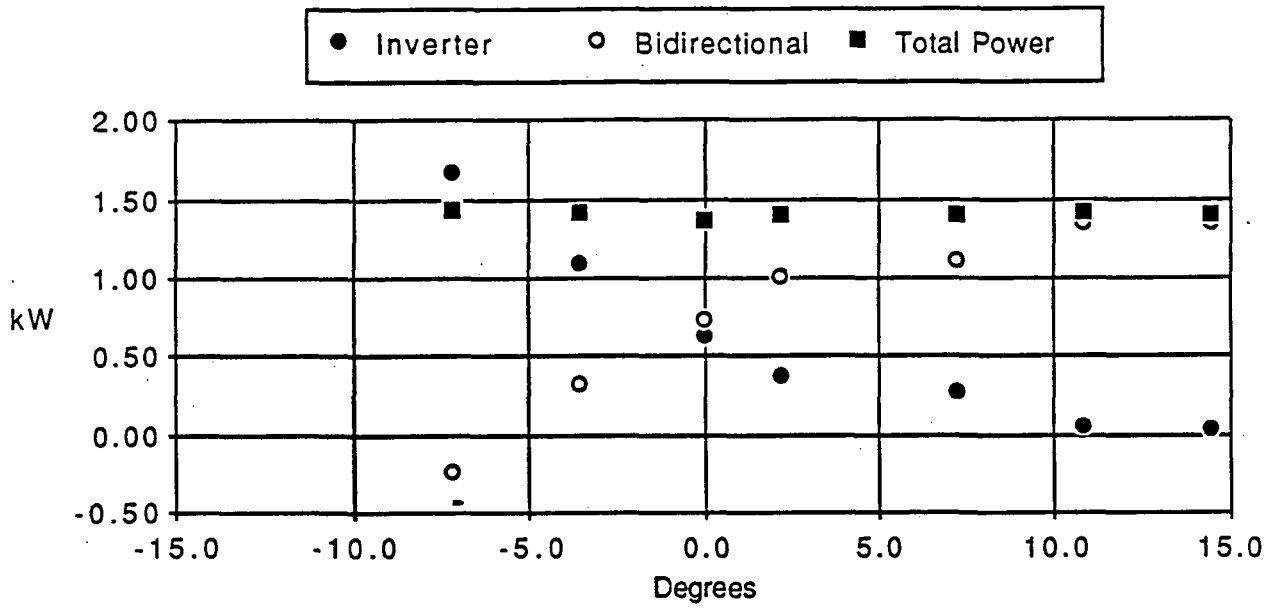

Figure 5-1. Power Output versus differential phase between Inverters and Bidirectional Receiver at 1.1-kW Load.

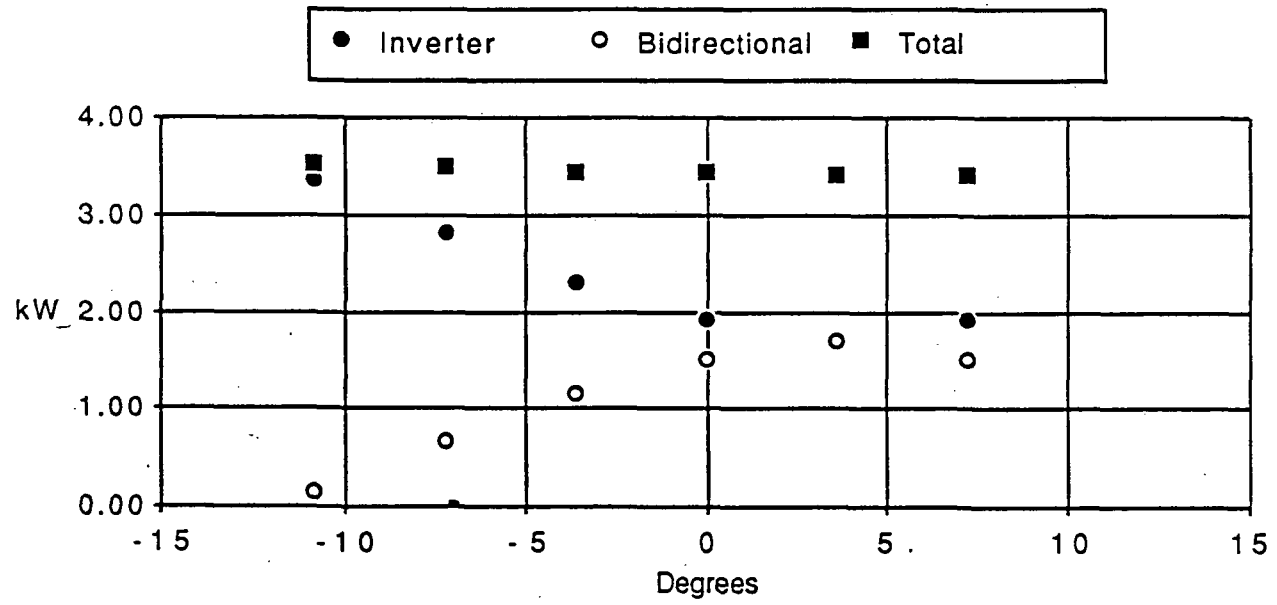

Figure 5-2. Power Output versus differential phase between Inverters and Bidirectional Receiver at 3.0-kW Load.

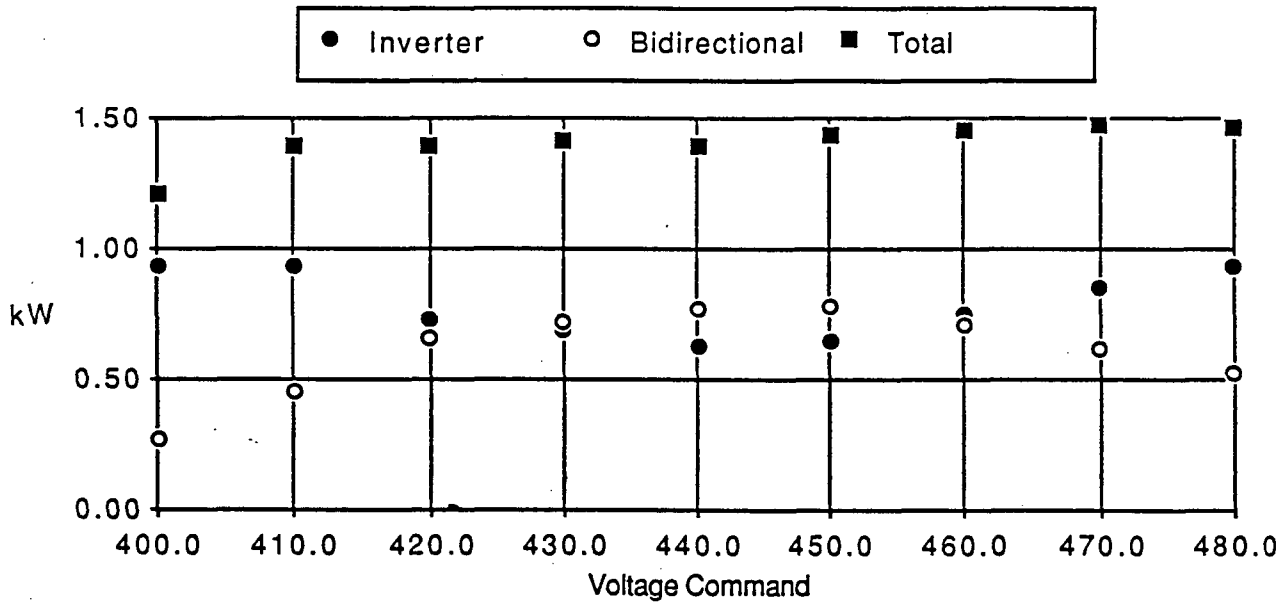

Figure 5-3. Power Output versus Bidirectional Receiver commanded Output Voltage at 1.1-kW Load.

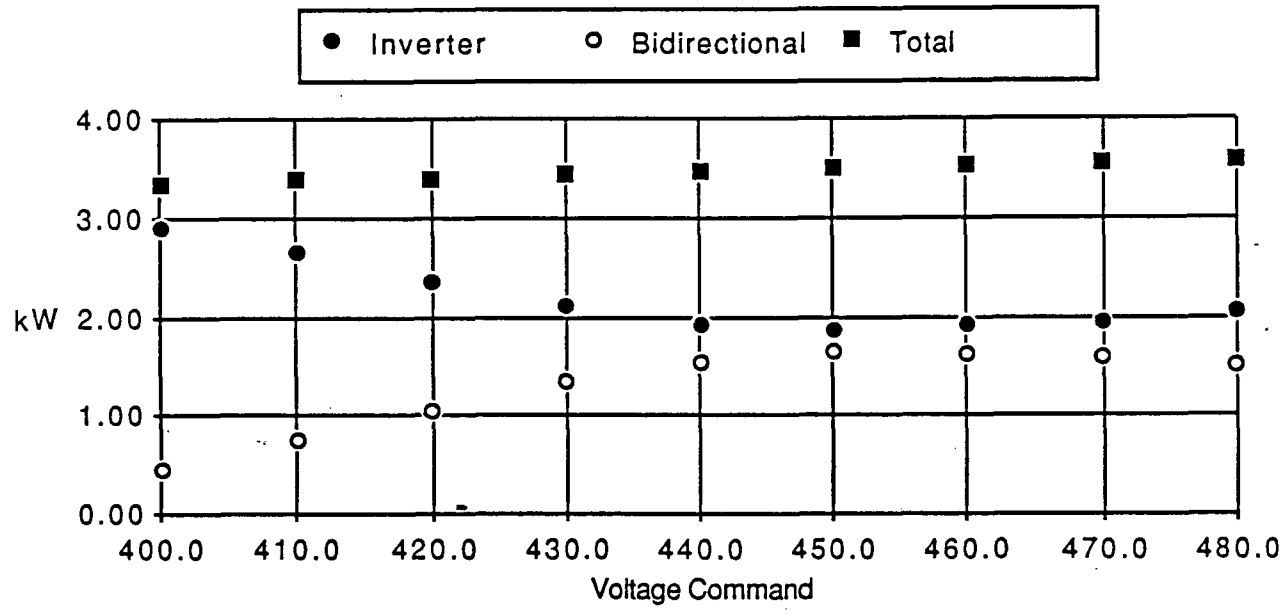

Figure 5-4. Power Output versus Bidirectional Receiver commanded Output Voltage at 3.0-kW Load.

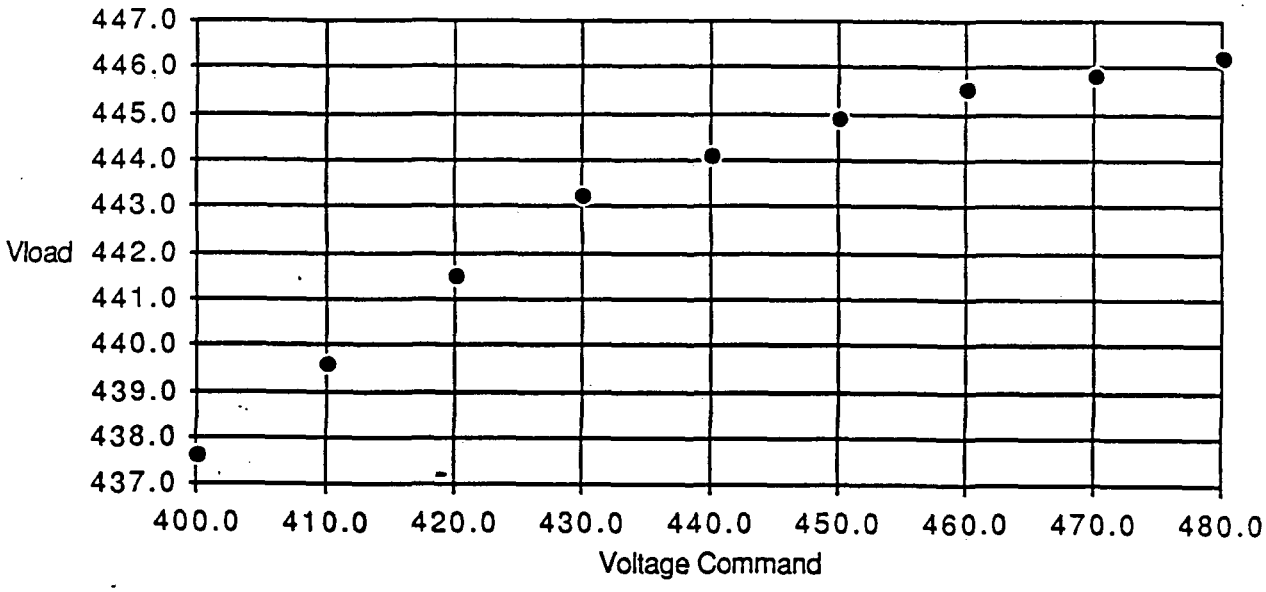

Figure 5-5 Voltage Output versus Bidirectional Receiver Commanded Output Voltage at 1.1-kW Load.

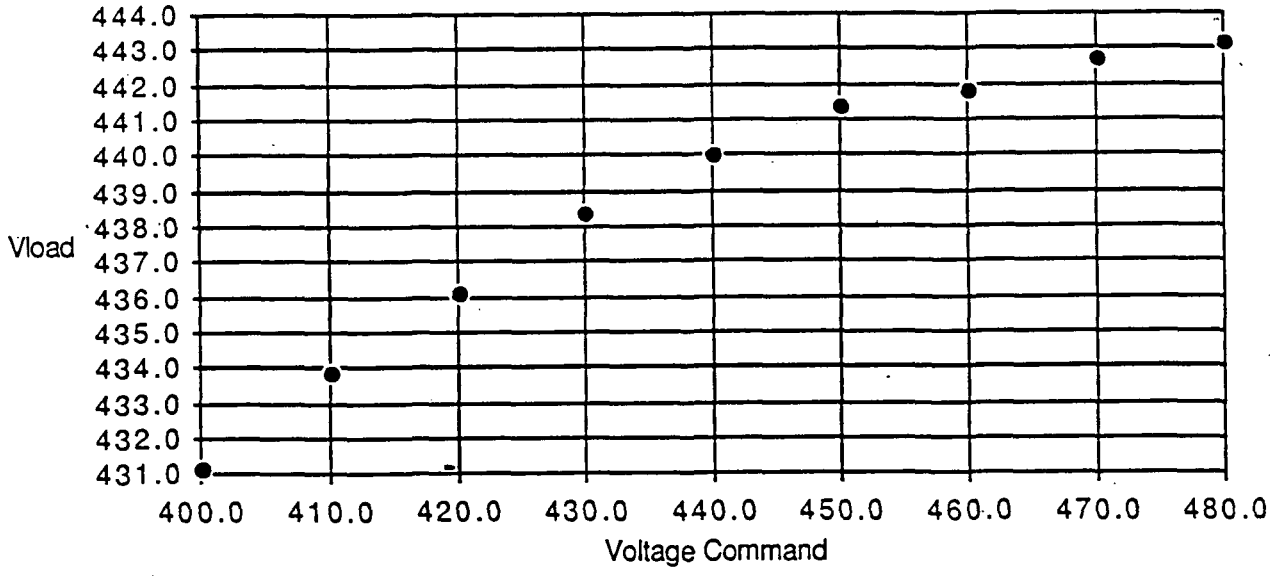

Figure 5-6. Voltage Output versus Bidirectional Receiver Commanded Output Voltage at 3.0-kW Load.

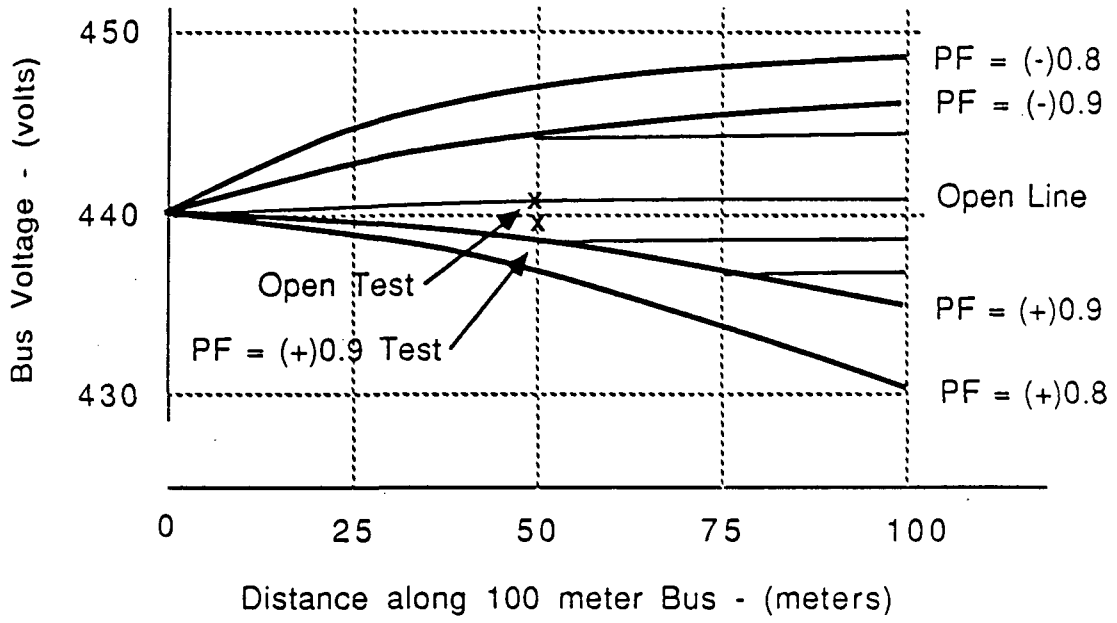

Figure 5-7. Bus voltages are stable and controlled.

The large total shunt capacitive kVA represented a 2.5 kVAR load to the 5kW MSFC testbed (50%). The 50% distribution system loading is unrealistic for the actual Space Station Power system. The actual Space Station EPS will initially be sized at 100 kW peak capacity, and will use transmission lines with similar characteristics as the Induction General transmission line characteristics listed in Table 5-1. The resultant stored energy in the Space Station distribution system will be a small percentage of the total power system capacity.

The current plan for the Space Station 20kHz bus is a single phase, stripline type transmission line which will have lower series inductance and resistance values than the MSFC bus. A prototype 20 kHz Space Station bus was designed and built by Induction General, and tested at General Dynamics as part of a separate contract. The bus was constructed with three flat litz wire conductors stacked on top of each other, separated by a insulating material. The middle conductor was the "hot" conductor and the two outer conductors were the returns. The bus was designed for 25 kVA @ 440 volts.

To evaluate the Induction General design, sending and receiving end bus voltage was measured for different loads on a 50 meter sample of the transmission line. The measurements were made using the NASA-LeRC 25 kW single phase 20kHz

breadboard. The transmission line series resistance, series inductance, and shunt capacitance values were calculated using the transmission line voltage drop formula for unity, lagging, and leading power factor loads and the results were in excellent agreement with the Induction General supplied values and are listed in table 5-1.

The data was supported by a computer analysis using the bus parameters for a 100 meter bus. The bus frequency response was calculated to be over 200 kHz. Since the 20-kHz line frequency is therefore at least an order of magnitude below the bus response, a valid model of the bus can be constructed using a series of lumped parameter sections. The computer analysis was run which used 5 meter sections and placed resistive, inductive, and capacitive loads at 25, 50, 75, and 100 meters. Figure 5-7 shows the results. The darker curves represent the locus of points for the various loads listed placed along the bus. The worst case occurs when the low power factor loads (±0.8) are connected at the end of the bus. The bus voltage is always within 10 volts of the nominal 440VAC, for a worst-case variation of less than 2.5%. The experimental data is about 50% lower than the calculated data, indicating greater damping in the actual system.

The results of both the computer analysis and the data confirm that 20 kHz power transmission behaves similar to 60 Hz power transmission as described in elementary power distribution textbooks: The voltage drop at the receiving end of the bus is positive for lagging power factor loads and negative for leading power factor loads, and varies as a function of the bus series resistance and inductance, the load power factor, and the load current. It is therefore reasonable to conclude that the 20-kHz bus voltage is well behaved and predictable, with the worst-case excursion from the nominal voltage less than ±2.5% for a 100 meter system of Induction General design, with no remote sensing or feedback. Using remote sensing, the Space Station power management processor could adjust the inverter output voltage according to the demand cycle to keep the user end voltage precisely at 440 volts, in a similar way that 60Hz utility companies compensate for transmission line voltage drops.

c. **Power Quality, Interference, and EMI** - Power quality and interference between the various users that might be connected to the distribution bus system is a function of the amount of current distortion (or conducted emissions) a user is allowed to "put back" onto the bus and the impedance (at the interference frequencies) of the inverters and bus supplying that user.

While not required by the MSFC program, these effects were evaluated on the LeRC

test program and the data is provided for completeness. The program evaluated voltage distortions for undistorted and highly distorted load currents to measure basic inverter distortion, interference levels, and output impedance as a function of frequency. The distortion data is summarized below:

- Basic inverter total harmonic distortion on the voltage is approximately 2.8% at full resistive load.
- Full receiver loads with no filtering add about 3.4% distortion at the inverter.
- Full receiver loads when properly filtered add only about 0.04% distortion.
- Low total source impedance near the 20-kHz power transmission frequency minimizes any effects from low order harmonic currents.

Output impedance characteristics were measured by comparing the magnitude of output voltage at the harmonic frequencies of interest with the load current at the same frequency. Figure 5-8 shows the magnitudes of the impedances at the low harmonic frequencies, plotted on the calculated values. The log magnitude scale on the abscissa is referred to 10 ohms. As you would expect, good agreement is evident at the lower frequencies. Experimental data and calculated values start to deviate from one another at the higher frequencies, where circuit strays not used in the model become more important.

A detailed EMI test was performed on the NASA-LeRC 20 kHz testbed to investigate the noise susceptibility of the inverter design as part of a separate contract. Bus current distortion measurements were taken which revealed that typical unfiltered receiver input currents exhibited about 30% distortion, with the high frequency current harmonics particularly significant (the 300 kHz harmonic was near 3% of the fundamental). The current distortion increased the inverter voltage distortion by about 3.4%, as should be expected because of the high inverter output impedance at the high frequencies. However, when simple filters were placed across the LeRC receiver inputs, the higher frequency current harmonics were significantly reduced (300 kHz dropped to 0.2%) which reduced the bus voltage distortion by almost the entire 3.4%. Thus, the inverter design is most susceptible to voltage distortion caused by high frequency current harmonics, which are easier to filter than the lower frequency current harmonics.

The MSFC testbed voltage distortion was measured to be 6% when loaded at 5kW with receiver loads. This was because the MSFC testbed receiver loads were not filtered. Although current distortion measurements were not taken on the MSFC testbed, the MSFC receivers are of similar design as the LeRC receivers, and the current distortion was similar to the unfiltered LeRC receiver current distortion. It should then be

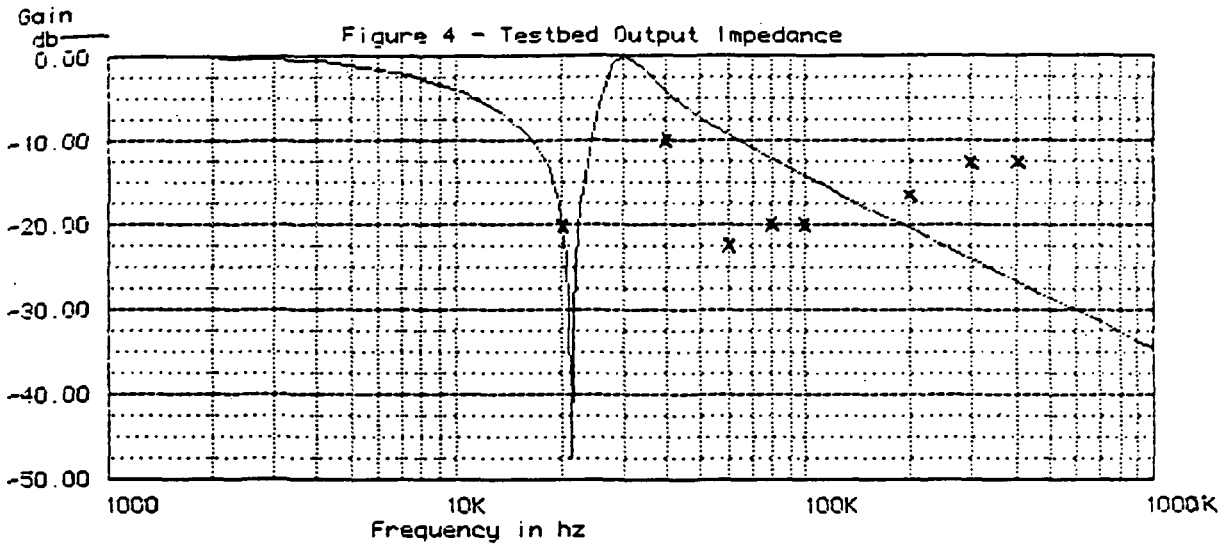

Figure 5-8. High-frequency inverter output impedance is low.

expected that the voltage distortion on the MSFC testbed should be close to the LeRC testbed distortion without filters on the receivers, which it is. It is recommended that this issue be investigated at MSFC by NASA engineers to verify these results.

The main significance of the EMI test data is that the basic 2.8% inverter distortion is not effected by load currents provided they are filtered properly. Since all Space Station loads will have to satisfy the Space Station EMI/EMC requirements for conducted emissions on the input power lines (which should keep the current distortion well below the 30% level measured on the testbeds), bus voltage distortions below the 3% level should be easily obtainable without significantly filtering the inverter output.

d. **Overloads and Short Circuits** - The system transient fault control was performed by the testbed RPC's. The RPC's react to overload current spikes and voltage drops, and shut down within 100 μs of a fault condition. The RPC fault protection capability was tested by placing overloads on the bus while the system was operating. After the overload was applied, the RPC's disconnected the inverters from the bus and isolated the fault.

Occasionally, an inverter SCR would commutate unintentionally and short the input power supply. This happened because the SCR's used as the main power switches in the inverters were susceptible to noise-induced turn-on, caused by voltage spikes, current spikes, and other phenomenon. Gate-cathode resistors and anode-cathode

snubber circuits were placed across each SCR which significantly reduced the turn-on problem. However, occasionally a system transient would result which still caused an SCR to commutate despite the noise-reduction circuits. Fuses were placed on the DC input to protect the SCR's in the few instances when the noise-reduction schemes were inadequate.

The actual Space Station inverters will use turn off switches which do not exhibit the inherent unintentional, noise-induced turn on problems of the SCR. Furthermore, the inverter gate drive circuits will incorporate a turn-off function which will turn each switch off before the next switch is fired, eliminating the possibility of two switches short circuiting the input. The most likely switch candidate is the new MOS Controlled Thyristors (MCT's) under development by General Electric for NASA-LeRC and the Air Force. Another candidate is the Insulated Gate Transistor (IGT). Both devices have similar properties including fast turn on & turn off times, high voltage rating, and low power MOS gate inputs. We are currently using the IGT's in our 20 kHz Motor Controller, developed under contract to NASA-LeRC. They have proven far superior in performance than the SCRs which were used in both the MSFC and the LeRC 20kHz testbed AC receivers. The AC receiver SCR's required extremely large and dissipative snubber networks to prevent dv/dt turn on; the IGT's on the motor controller have no dissipative snubber networks and do not commutate unless a gate drive signal is received.

The breadboard demonstrated that the inverter can limit steady state overloads through the active phasor regulation loop. A current limit phasor regulation loop provides positive control of the output current, and has a response time of approximately 30 milliseconds. The current control function is an analog loop, with computer controlled references, which allow for different fault control modes:

- Hard limit the fault current, and shift critical loads to another bus
- Computer or operator can elect to raise the limit and continue to power the loads
- Computer or operator can elect to raise the limit to a value high enough to burn out the fault, in an attempt to clear it.

Transient limiting, above the frequency response of the regulator loop will be provided by the series output capacitor in the final Space Station design. A Maphan resonant inverter can operate continuously from open to short circuit with proper selection of the series output capacitor. Its value is selected to allow the bridge to continue to operate by keeping the natural resonant frequency safely above 20kHz even if the output is

shorted.

e. **Low Power Factor Loads** - Since low power factor loads usually reflect into the resonant network for this class of power processors, previous designs were intolerant of that type of load. This breadboard's extrapolation of the basic technology resonant technology accommodates low power factor loads as follows:

Capacitive Loads:

- Are isolated by the series output capacitor.
- Frequency Effects are limited by the value of the series output capacitor, since adding capacitance in series results in lower total capacitance seen by the resonant network.
- There is no effect until the capacitive loads are large enough to become overloads and are actively limited by the regulation loop current limit.

Inductive Loads:

- Are partially isolated by the series output capacitor.
- Since an inductor is effectively a minus capacitor, it can effectively reduce the value of the series output capacitor, and if large enough, cancel its isolation and change the natural resonant frequency. A higher natural frequency increases output distortion. In the breadboard, the capacitor is sized so that there are no frequency effects above Power Factors of 0.7
- Testing has shown that for very low inductive power factors (less than 0.5), possible driver logic inhibits can cause output failures.

6.0 Deliverables

6.1 Documentation

6.1.1 Final report covering system development
6.1.2 Operations and service manuals
6.1.3 System software with backup copies
6.1.4 Schematics and parts lists
6.1.5 System photographs and transparencies
6.1.6 Software flowcharts and listings
6.1.7 Acceptance test plan
6.1.8 Acceptance test procedure
6.1.9 Acceptance test data
6.1.10 All other pertinent documentation
6.1.11 Documentation sufficient to ensure ease of operation, maintenance, and repair of entire system by MSFC personnel

6.2 Hardware

The following specific items, called out by the latest contract revision, comprise the AC Power System Breadboard of this contract and were delivered to NASA Marshall Space Flight Center in December of 1987.

6.2.1 Inverter/transformer (driver) module(s) with these characteristics:

- 3 phase or 1 phase
- 440 Vac rms ±5%
- 20 kHz ±1%
- ≥ 5 kW
- Standard utility source (220 or 440 Vac, 3Ø) or 200 Vdc

6.2.2 Power busses (2) parallel with these characteristics:

- Share loads under normal conditions
- Each bus capable of supplying full load
- Each bus at least 15 meters in length

6.2.3 User load modules (5):

6.2.3.1 First load module (400 Hz, three-phase receiver)

- 120/208 Vac rms ±5%
- 400 Hz ± 5.3%
- 3 phase
- 1 kW

6.2.3.2 Second load module (Single-phase, ac receiver)

- 120 Vac rms ±5%
- 60 Hz ±1% or 400 Hz ±5.3%
- 1 phase
- 500 W

6.2.3.3 Third load module (Variable-frequency, ac receiver)

- 120/108 Vac rms ±5%
- 800 or 1200 Hz Table of Freqs
- 3 phase
- 1 kW

6.2.3.4 Fourth load module (DC receiver)

- 28 Vdc ±1 Vdc
- 1 kW

6.2.3.5 Fifth load module (Bidirectional)

- 1 kW
- Receiver mode—150 Vdc battery charger
- Driver mode
  a. battery input (150 Vdc simulator)
  b. Output
    - 440 Vac ±5%
    - 20 kHz ±1%
    - 3 phase
    - Synchronized with power bus

6.2.4 Control and fault isolation switch matrices:

- Load: Capable of managing combination of 2 busses and 5 load modules under control of microprocessor based controller
- Driver: Under control of microprocessor based controller

6.2.5 Fault tolerance:

- Fail safe, fail operational
- Possible faults: User, user switch, bus, bus switch, inverterFaults isolated by switch matrices

6.2.6 Microprocessor controller(s):

- Include appropriate interfaces for I/O of data for human operator to utilize. As a minimum: Keyboard, CRT, and printer integrated with system
- Graphic-oriented operator interface program

6.2.7 Miscellaneous system requirements:

- System shall be modular in form
- System capable of running with any combination of modules removed
- Allowable power factor 0.8 lagging to 0.8 leading
- Capable of running continuously at full power
- All hardware mounted in sturdy, durable enclosures
- Hardware quality and durability for several years of safe and reliable operation
- Ease of system maintainability shall be a system goal
- Adequate spares of custom piece parts and documentation to enable procurement by MSFC personnel

6.2.8 Requirements review:

- At beginning of contract period
- Mid-term review

6.2.9 Activities at MSFC:

- Acceptance testing at MSFC or contractor site as agreed
- ATP to be witnessed and approved by MSFC technical manager or representative(s)
- Install/checkout/demonstrate at MSFC
- One to two weeks of training in operation and maintenance at MSFC

6.2.10 Miscellaneous deliverable items:

- AC processing system
- All physical enclosures and supports
- All necessary cables and connectors

6.3 Installation and Checkout at Marshall Space Flight Center

Installation and checkout of the hardware was accomplished in the AC Power System test facility at Marshall Space Flight Center by NASA personnel, with assistance, as required, from General Dynamics/Space Systems Division, Space Power Systems engineering personnel. This has been verified by successful completion of the final acceptance test in the NASA facility.

7.0 Conclusions and Recommendations

7.1 Conclusions

The following are the significant conclusions about this hardware, as demonstrated by this development, construction, and test program. They are divided into sections for each major breadboard hardware element, and include the program's major accomplishments and lessons learned for each.

7.1.1 Inverters

The significant hardware developments that were proven in this program are:

- Overload control
- Regulation
- Output impedance control and its effects on interference
- Distortion and EMI/EMC compatibility
- Paralleling and current sharing
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Turn-off type switches offer significant improvements in operation and performance in the areas of, efficiency, reliability, and control.
- Regulator designs must be improved to include better line regulation and positive control of current sharing.
- Resonant network designs must be compensated to accommodate the maximum phasor separation at maximum load and maximum input voltage.
- Maximum efficiency occurs at full load

7.1.2 Bus Control Switch Matrix and Load Control Switch Matrix

The significant hardware developments that were proven in this program are:

- Remote Power Controller demonstration
- Overload control
- Less than 100-μsecond response
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Turn-off type switches offer modest improvements in operation and performance for

efficiency, reliability, and control.

- Semiconductor switch capacitance is an important design consideration for reactive load isolation.
- Load Power Factor effects drive thyristor design implementations toward DC drives with synchronized turn on and turn off.

7.1.3 Transmission Lines

The significant hardware developments that were proven in this program are:

- Definition and identification of configuration dependent characteristics
- Regulation and stability demonstration
- Line impedance control and its effects on interference
- Distortion effects and EMI/EMC compatibility

Lessons learned which impact future hardware designs are:

- Stripline or flat configurations offer the best control of characteristics for long lines.
- Capacitance effects can be compensated, if necessary.
- High surface area configurations (Litz wire or foils) should be used to minimize losses in long lines.
- Conventional wiring can be used for short (inside station modules or units) interconnections.

7.1.4 Bidirectional Receivers

The significant hardware developments that were proven in this program are:

- Overload control (in both directions)
- Phase delay regulation (as a receiver)
- Output impedance control and its effects on interference (when used as a source)
- Distortion and EMI/EMC compatibility, both when used as a source and reflected to the line when supplying a load
- Paralleling and current sharing with Inverters (when used as a source)
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Same as inverters when used as a source (see Paragraph 7.1.3).
- Control of clock phase is required for different sources, either with positive phase control of a master clock input, or with a phase-locked loop, synchronized to the line.
- Clock phase can be used to control the operational mode, and change the character of

the receiver's operation from source to load.

7.1.5 DC Receivers

The significant hardware developments that were proven in this program are:

- Overload control
- Phase-delay regulation
- Transformer-Rectifier-Filter configuration verified
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- A critical value output inductor is required for 20-kHz input current control.
- A flyback diode is required to prevent the output filter from reflecting its power factor to the input.

7.1.6 Three-Phase AC Receivers

The significant hardware developments that were proven in this program are:

- Overload control
- Regulation
- Basic motor control verified
- Distortion and EMI/EMC compatibility is controlled for the three phase configuration
- Twelve-step configuration (two-on/one-off and three-on states)
- Computer control capability and algorithms

Lessons learned which impact future hardware designs are:

- Pulse population modulation provides improved control and frequency resolution for the AC outputs.
- Phase delay regulation is possible and reasonable if pulse population does not have sufficient resolution.
- Population and regulation control approaches which use an AC reference voltage provide improved low frequency AC output control.

7.2 Recommendations

7.2.1 Breadboard Related

a. Upgrade the breadboard to include hardware (especially for the inverters) that incorporates turn-off type devices for the main power switching components. Use MCTs, IGTs, FETs, or bipolar transistors instead of SCRs, to improve efficiency and simplify drive and protection circuitry.

b. Upgrade the breadboard regulator control boards to newer designs which include clock phase control for positive control of current sharing, and improved gain characteristics for improved bus voltage control performance.

7.2.2 Generic 20-kHz Hardware Related

a. Where possible hardware designs (especially for the inverters) that incorporate turn-off type devices for the main power switching components should be used. Use MCTs, IGTs, FETs, or bipolar transistors instead of SCRs, to improve efficiency and simplify drive and protection circuitry.

b. High surface area wiring configurations (Litz wire or flat foils) should be used to compensate for skin effect in long power busses to minimize losses and/or conductor mass. Flat braid or stripline configurations provide the best management and control of line parameters. Conventional wiring may be used for short runs (inside modules or units) or low power applications. Twisted pair configurations will minimize interference and pickup in these conventional wiring applications.

c. Remote Power Controllers and Remote Bus Isolators — must be designed to accommodate very low power factor loads, even though spec limits on users normally would control input power factors. Connecting to an unloaded power bus is probably the worst case (power factor < 0.1), even though it is a small load.

d. EMI/EMC — The intent of the classical EMI/EMC specifications (such as MIL-STD-461 and MIL-STD-462) should be applied to load interface hardware attached to the 20-kHz power bus. When they are required, the vehicle system power quality should be in the 3% total harmonic distortion range.

e. Transformers — Non-linear elements (switches, rectifiers, etc.) and transients in utility

systems of this type can often cause AC unbalances which appear as a net DC term in the current. Therefore, even though this is an all AC system, transformers and other magnetic components should be designed to accommodate some reasonable percentage of DC to avoid saturation effects.

8.0 References

1 **"An SCR Inverter with Good Regulation, Sine-Wave Output"**; Neville Mapham; IEEE Transactions on Industry and General Applications; IGA-3, No.2, Apr-May, 1967.

2 **"Bidirectional Power Converter Control Electronics"** , Final Report; NASA CR 175070, NAS 3-23878; J.W.Mildice, General Dynamics - Space Systems Division.

3 **"Study of Power Management Technology for Orbital Multi-100kWe Applications"**; Final Report, NASA CR 159834; J.W.Mildice, General Dynamics, Convair Division

4 **"Study of Multi-Megawatt Technology Needs for Photovoltaic Space Power Systems"**; Final Report, NAS 3-21951; D.M.Peterson, General Dynamics, Convair Division

5 **"20-kHz, Proof of Concept Test Program"**; Final Report, NAS 3-22777; Loran J. Wappes, General Dynamics - Space Systems Division

6 **"Fault Tolerant AC Power Processing"**; Final Report, GDC-ERR-83-212; Loran J. Wappes, General Dynamics - Convair Division, December, 1983

7 **"Control Considerations for High-Frequency, Resonant Power Processing Equipment Used in Large Systems"**; J. W. Mildice, Proceedings of the IECEC, August 10-14, 1987 (NASA Technical Memorandum 98226; AIAA-87-9353)

8 **"Performance Test Report, LeRC AC Power System Testbed"**; Contract NAS 3-23878; R. Sundberg, General Dynamics - Space Systems Division, November, 1987

9 **"Acceptance Test Report for 20-kHz Power Testbed"**; Contract NAS 3-24399; Frederick J. Wolf, NASA LeRC, 30 September, 1987

10 **"Bidirectional Four Quadrant (BD4Q) Power Converter Development"**, Final Report, NASA CR 159660, F.C.Schwarz, Power Electronics Assoc. Inc.

11 **"Controllable Four-Quadrant AC to DC and AC Converter Employing an Integral High Frequency Series Resonant Link"**; U.S.Patent 4,096,557, June, 1978

12 **"A Practical Resonant Converter Using High Speed Power Darlington Transistors"**; Sridar R. Babu, General Electric Co., Auburn, NY, PCI March, 1982 Proceedings, pp 122-141

13 **"Advances in Series Resonant Inverter Technology and Its Effect on Spacecraft Employing Electric Propulsion"**; R.R.Robson, Hughes Research Labs, Malibu, CA, presented at AIA/UASS/OGLR 16th International Electric Propulsion Conference, November, 1982.

14 **"AC Power System Testbed Final Report"**; J. Mildice and R. Sundberg, General Dynamics/Space Systems Division, San Diego, CA, November 1987.

Appendix A

Work Statement

AC POWER SYSTEM BREADBOARD
STATEMENT OF WORK

The contractor shall provide the personnel, materials, facilities, and equipment to perform the following task:

Develop and deliver to MSFC a five (5) kilowatt alternating current (ac) high voltage, 20 kHz, three phase power processing system. This system shall be modular in form with various driver and receiver module plus associated equipment as described below and depicted in Figure 1.

The inverter/transformer (driver) module(s) shallbe capable of continuously delivering an output ac voltage of 440 Vac rms with ± 5% voltage regulation, 20kHz frequency (±1% frequency regulation), three phase with total output power equal to or greater than five (5) kW. The output power shall be delivered to two (2) parallel power busses which shall share the loads under normal operating conditions, with each bus capable of supplying the full load requirement when operating alone. The driver modules shall employ a standard utility source (220 or 440 Vac, 3Ø).

The system shall employ five (5) user modules, each capable of delivering one (1) kW output power. The system shall be capable of running with any comibnation of modules removed. The first module shall deliver 120/210 Vac rms (± 5%) , 400 Hz (±1%), 3 phase power. The second module shall deliver 120 Vac rms (±5%), 60 Hz(±1%), single phase. The third module shall deliver 120.208 Vac rms (±5%) at either 800 or 1200 Hz (±1%), three phase. The fourth module shall deliver 28Vdc (±1Vdc). The fifth module shall be a bi-directional receiver/driver module, capable of operating as a 150Vdc receiver (user) module to function as a battery charger or as a system driver/inverter module operating from a charged battery to put power back onto the user module input bus(ses) at 440Vac (±5% regulation), 20kHz (±1%), three phase, synchronized with the power bus. The primary power distribution busses shall each be at least 15 meters in length. The allowable power factor range of the system at all loads shall be 0.5 lag to 0.8 lead.

This system shall be capable of running continuously at full power. It shall contain a system integrated load control and fault isolation switch matrix, capable of managing the combination

of two main power busses and five load modules, under the control of a microprocessor based controller (included in the system).

The system shall also contain a driver module(s)/bus control and fault isolation switch matrix under control of a microprocessor based controller (included in the system).

The system shall be fault tolerant to the extent that the system is expected to respond in a fail safe, fail operational manner. Possible faults include user faults, user switch faults, bus faults, bus switch faults, and inverter faults. Faults shall be isolated from the system by the fault isolator switch matrices.

The system shall include all hardware mounted in appropriate sturdy, durable enclosures. The micorprocessor(s) for controlling the system shall include appropriate interfaces for input/output of data for the human operator to utilize. This shall include, as a minimum, a keyboard, CRT, and printer integrated with the system. All hardware shall be to such quality and durability to support several years of safe and reliable operation.

A requirements review at the beginning of the oontract period as well as a mid-term review shall be held with the contractor and MSFC personnel. Acceptance testing shall be conducted at MSFC or the contractor site as agreed upon between the two parties. This testing shall be witnessed and approved by the MSFC technical manager and/or his representative(s). Regardless of the acceptance testing site, the contractor shall install, checkout, and demonstrate the entire system at MSFC and shall then provide one to two weeks of training in the operation and maintenance of the system to MSFC personnel at MSFC. Ease of system maintainability shall be a system goal. Adequate spares of custom piece parts shall be provided to MSFC along with adequate documentation enabling procurement of such parts by MSFC personnel.

Deliverable items in addition to the ac processing system shall include all physical enclosures and supports, all necessary cables and connectors, a final report covering system development, operations and service manuals, system software with backup copies, schematics parts lists, system photographs and transparencies, software flow-

charts and listings, acceptance test plan/procedure with test data, and all other pertinent documentation. Documentation shall be sufficient to ensure ease of operation and maintenance and repair of the entire system by MSFC personnel.

AC BREADBOARD

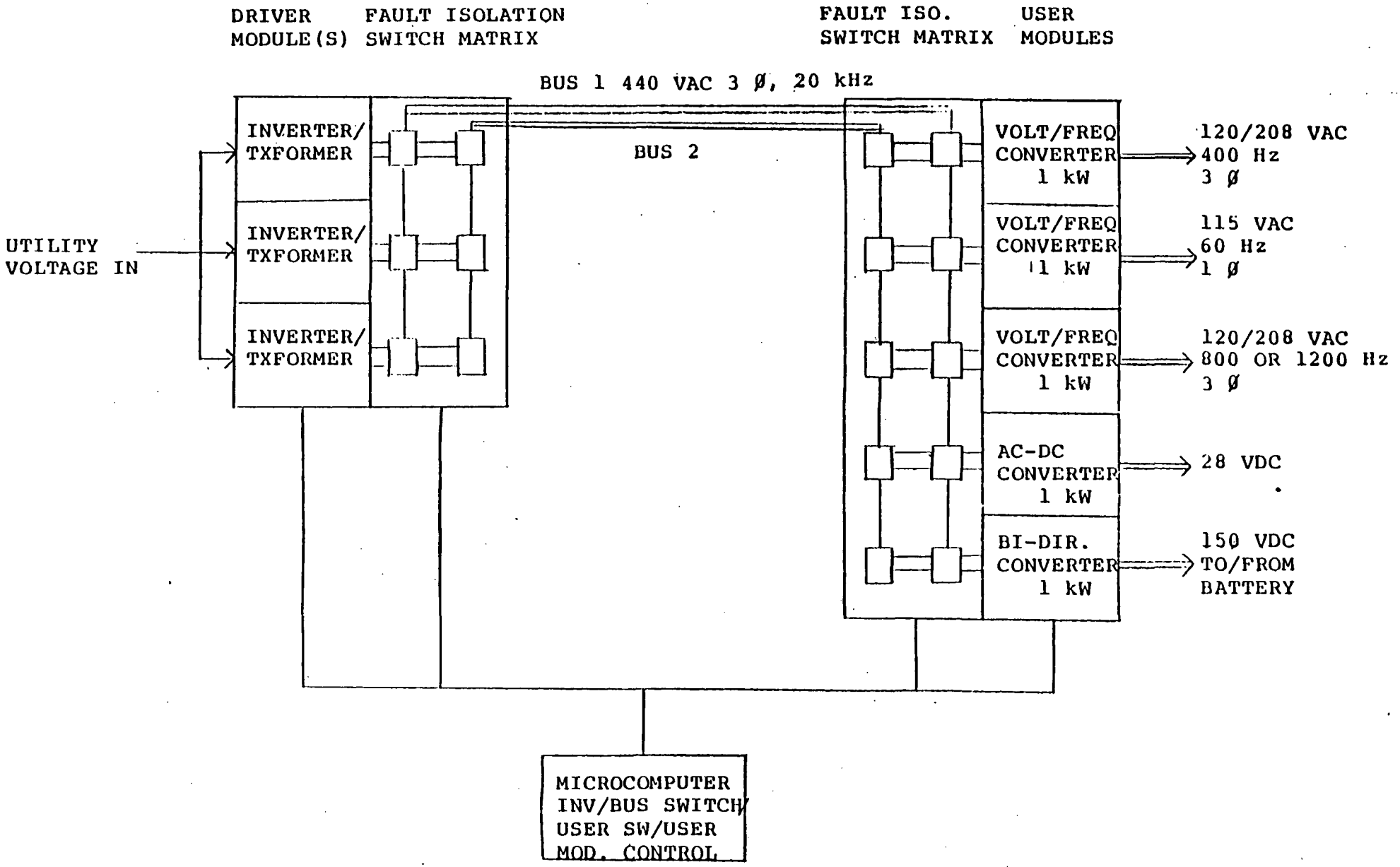

FIGURE 1.

Appendix B

Hardware/Software Requirements Digest

Original Requirement	Updated Requirement
Inverter/transformer (driver) module(s):	
3 phase	or 1 phase
440 Vac rms ±5%	
20 kHz ±1%	
≥ 5 kW	
Standard utility source (220 or 440 Vac, 3Ø)	or 200 Vdc
Power busses (2) parallel:	
Share loads under normal conditions	
Each bus capable of supplying full load	
Each bus at least 15 meters in length	
User load modules (5):	
First load module	
120/208 Vac rms ±5%	
400 Hz ±1%	Any frequency from table ±1%
3 phase	
1 kW	
Second load module	
120 Vac rms ±5%	
60 Hz ±1%	Any frequency from table ±1%
1 phase	
1 kW	500 W
Third load module	
120/108 Vac rms ±5%	
800 or 1200 Hz ±1%	Any frequency from table ±1%
3 phase	
1 kW	
Fourth load module	
28 Vdc ±1 Vdc	
1 kW	

Original Requirement	Updated Requirement
Fifth load module — bidirectional	
1 kW	
Receiver mode:	
150 Vdc battery charger	
Driver mode:	
battery input (150 Vdc simulator)	
440 Vac ±5%	
20 kHz ±1%	
3 phase	
Synchronized with power bus	
Control and fault isolation switch matrices:	
Load:	
Capable of managing combination of 2 busses and 5 load modules	
Under control of microprocessor based controller	
Driver:	
Under control of microprocessor based controller	
Fault tolerance:	
Fail safe, fail operational	
Possible faults: User, user switch, bus, bus switch, inverter	
Faults isolated by switch matrices	
Microprocessor controller(s):	
Appropriate interfaces for I/O of data for human operator to utilize. As a minimum: Keyboard, CRT, and printer integrated with system.	
Graphic-oriented operator interface program	Requirement added
Misc. system requirements:	
System shall be modular in form	
System capable of running with any combination of modules removed	
Allowable power factor 0.5 lag to 0.8 lead	0.8 lag to 0.8 lead
Capable of running continuously at full power	

Original Requirement

Updated Requirement

All hardware mounted in sturdy, durable enclosures
Hardware quality and durability for several years of safe and reliable operation
Ease of system maintainability shall be a system goal
Adequate spares of custom piece parts and documentation to enable procurement by MSFC personnel

Requirements review:

At beginning of contract period
Mid-term review

Activities at MSFC:

Acceptance testing at MSFC or contractor site as agreed
ATP to be witnessed and approved by MSFC technical manager or representative(s)
Install/checkout/demonstrate at MSFC
One to two weeks of training in operation and maintenance at MSFC

Deliverable items:

AC processing system
All physical enclosures and supports
All necessary cables and connectors
Final report covering system development
Operations and service manuals
System software with backup copies
Schematics and parts lists
System photographs and transparencies
Software flowcharts and listings
Acceptance test plan
Acceptance test procedure
Acceptance test data
All other pertinent documentation
Documentation sufficient to ensure ease of operation, maintenance, and repair of entire system by MSFC personnel

Appendix C

Electrical Hardware Schematics

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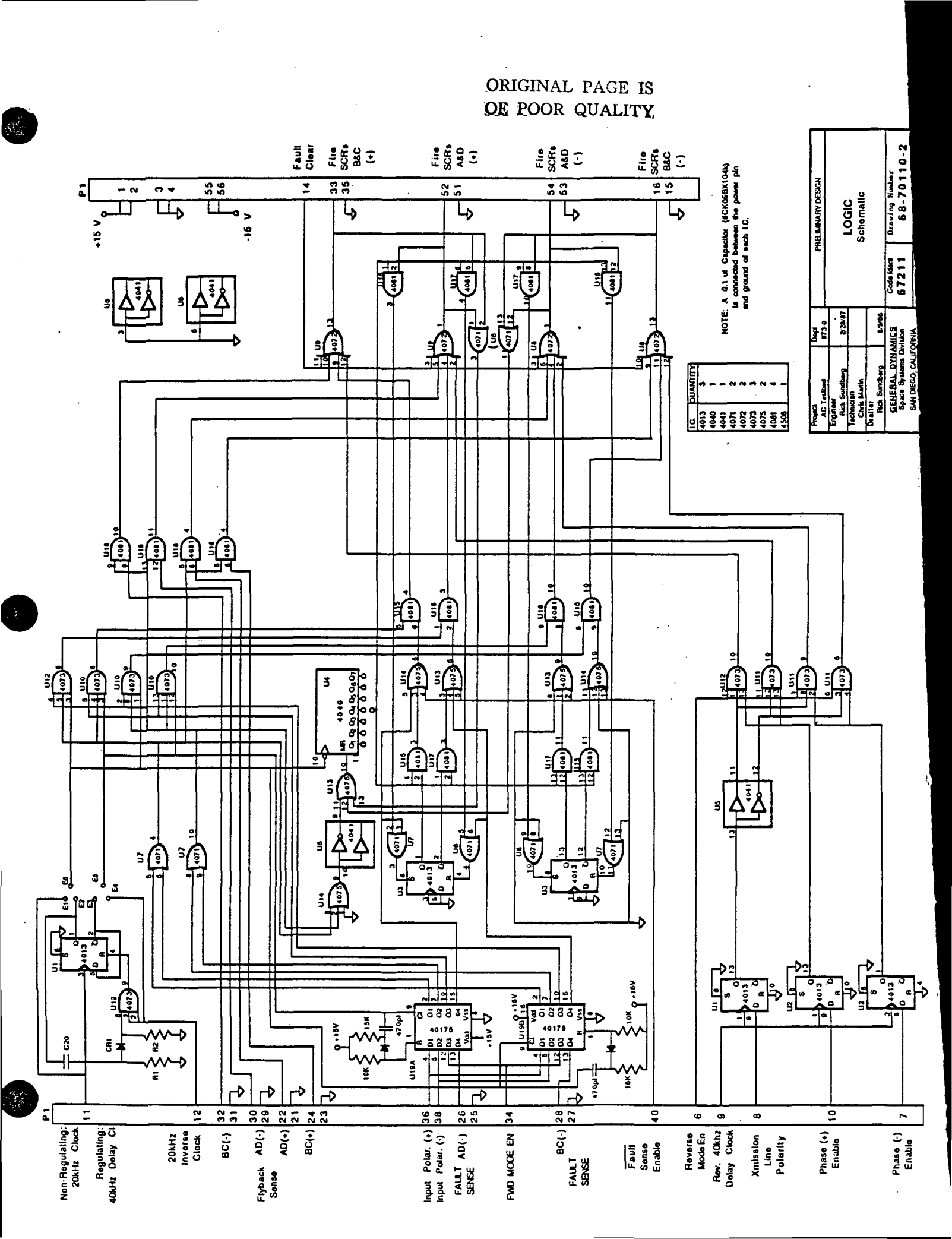
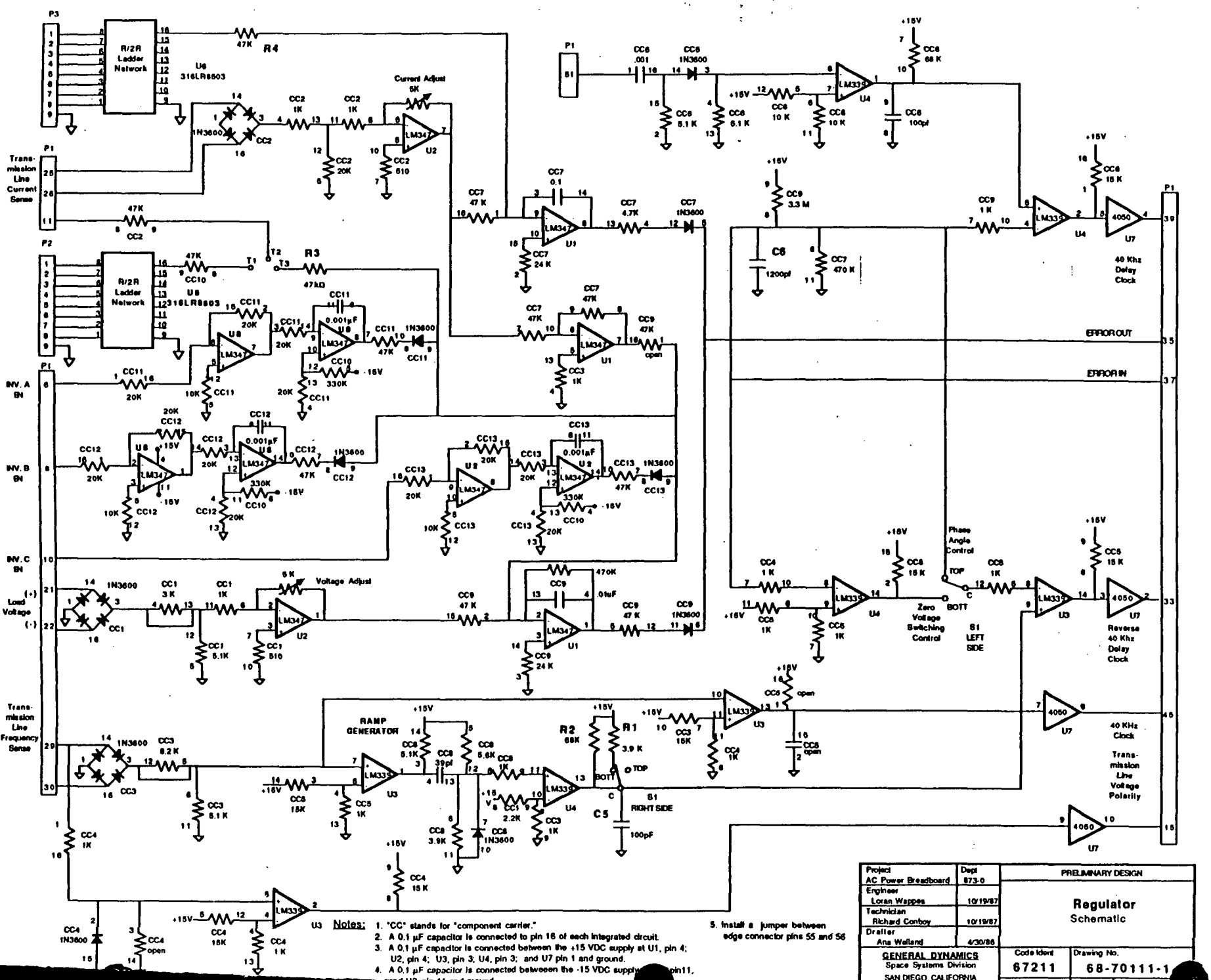
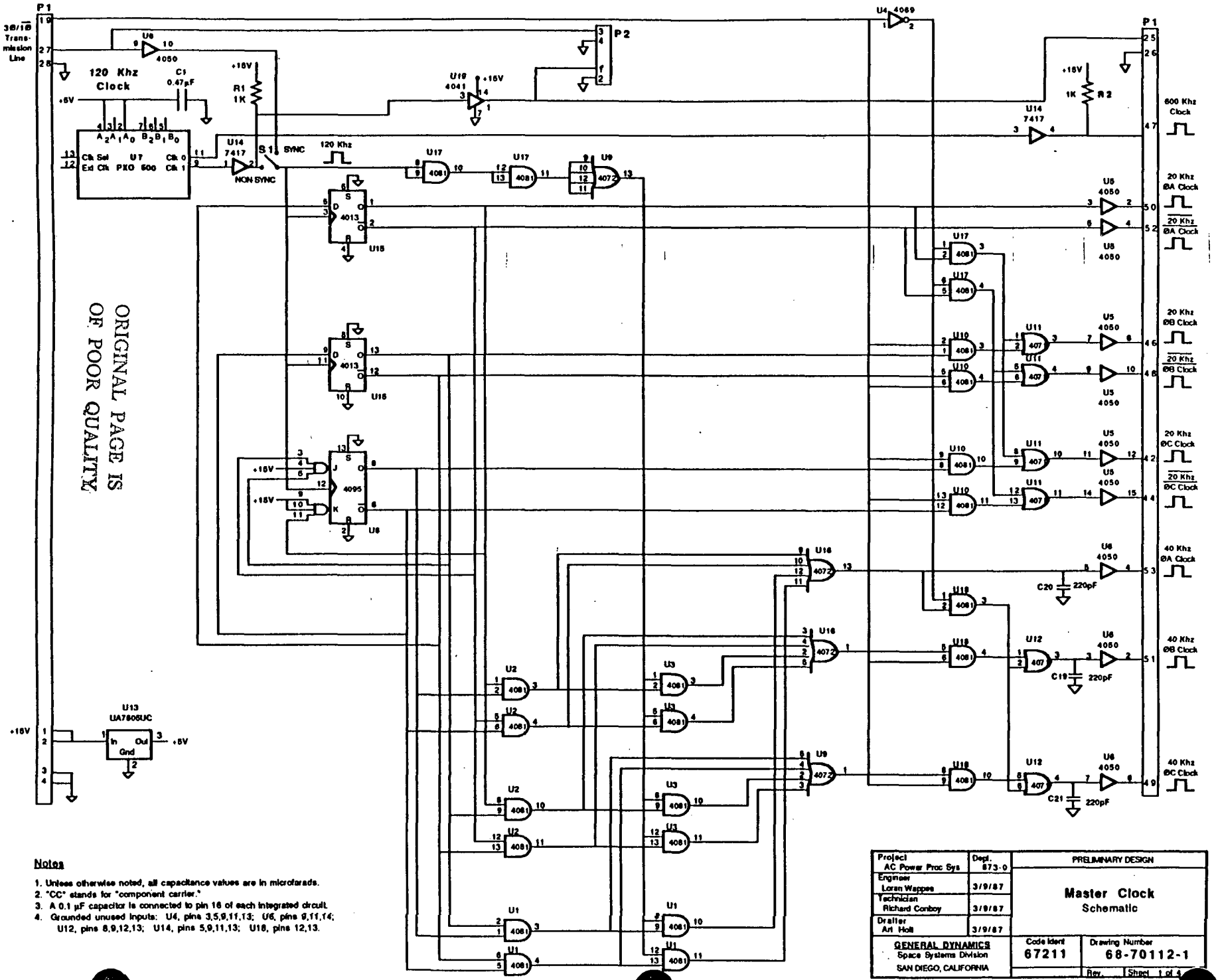




Project: AC Power Breadboard	Dept: 873-0	PRELIMINARY DESIGN	
Engineer: Loran Wappes	10/19/87	Regulator Schematic	
Technician: Richard Conboy	10/19/87		
Drafter: Ana Welland	4/30/88		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA		Code Ident: 67211	Drawing No.: 68-70111-1
			Rev / Sheet 1 of 1



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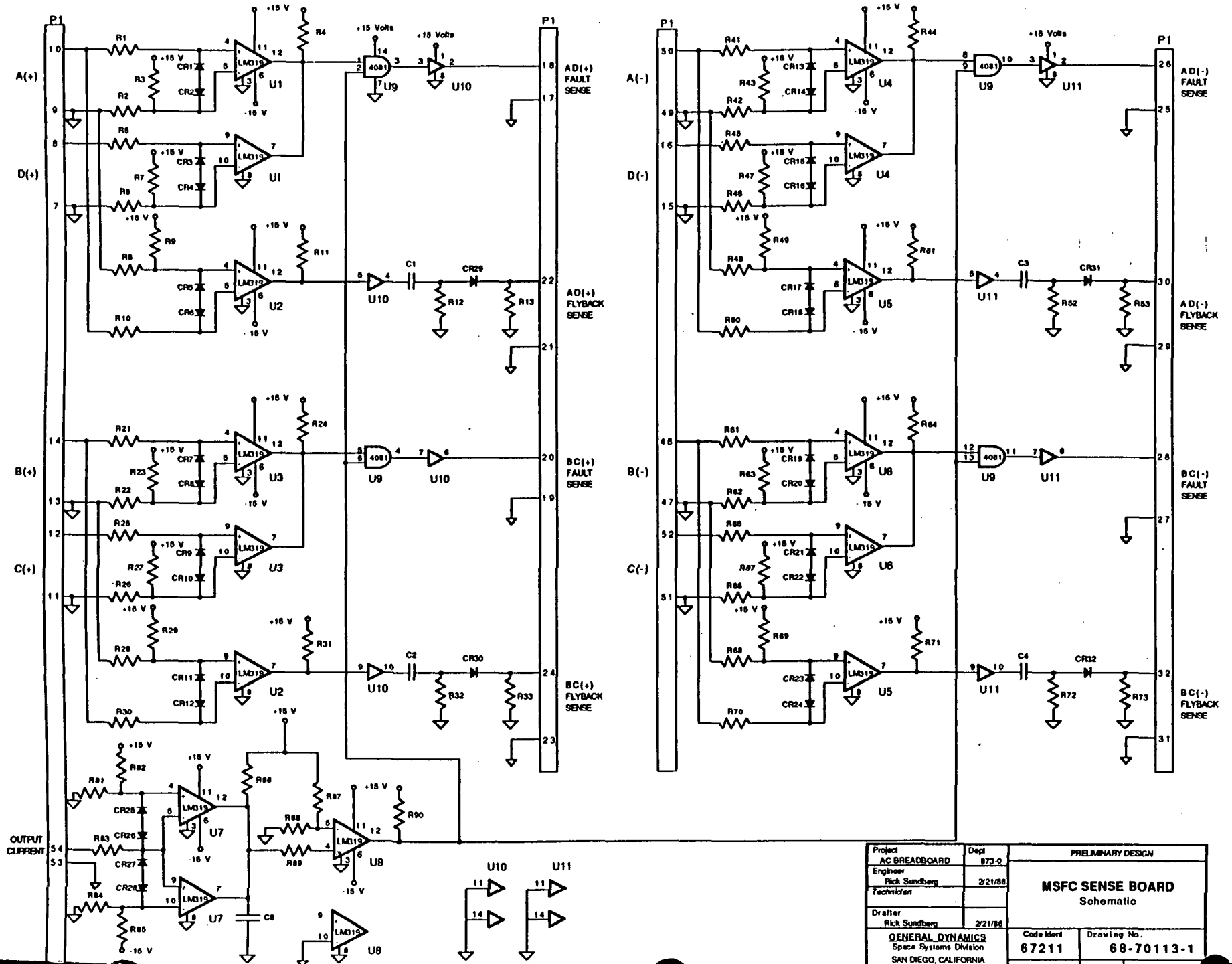
Notes

1. Unless otherwise noted, all capacitance values are in microfarads.
2. "CC" stands for "component carrier."
3. A 0.1 μF capacitor is connected to pin 16 of each integrated circuit.
4. Grounded unused inputs: U4, pins 3,5,9,11,13; U6, pins 9,11,14; U12, pins 8,9,12,13; U14, pins 5,9,11,13; U18, pins 12,13.

Project: AC Power Proc Sys	Dept. 873-0	PRELIMINARY DESIGN
Engineer: Loren Wappes	3/9/87	Master Clock Schematic
Technician: Richard Conboy	3/9/87	
Drafter: Art Holt	3/9/87	
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA	Code Ident 67211	Drawing Number 68-70112-1
		Rev. Sheet 1 of 4



Project: AC BREADBOARD	Dept: 873-0	PRELIMINARY DESIGN	
Engineer: Rick Sundberg	2/21/86	MSFC SENSE BOARD Schematic	
Technician:			
Drafter: Rick Sundberg	2/21/86		
GENERAL DYNAMICS Space Systems Division SAN DIEGO, CALIFORNIA		Code Ident: 67211	Drawing No.: 68-70113-1

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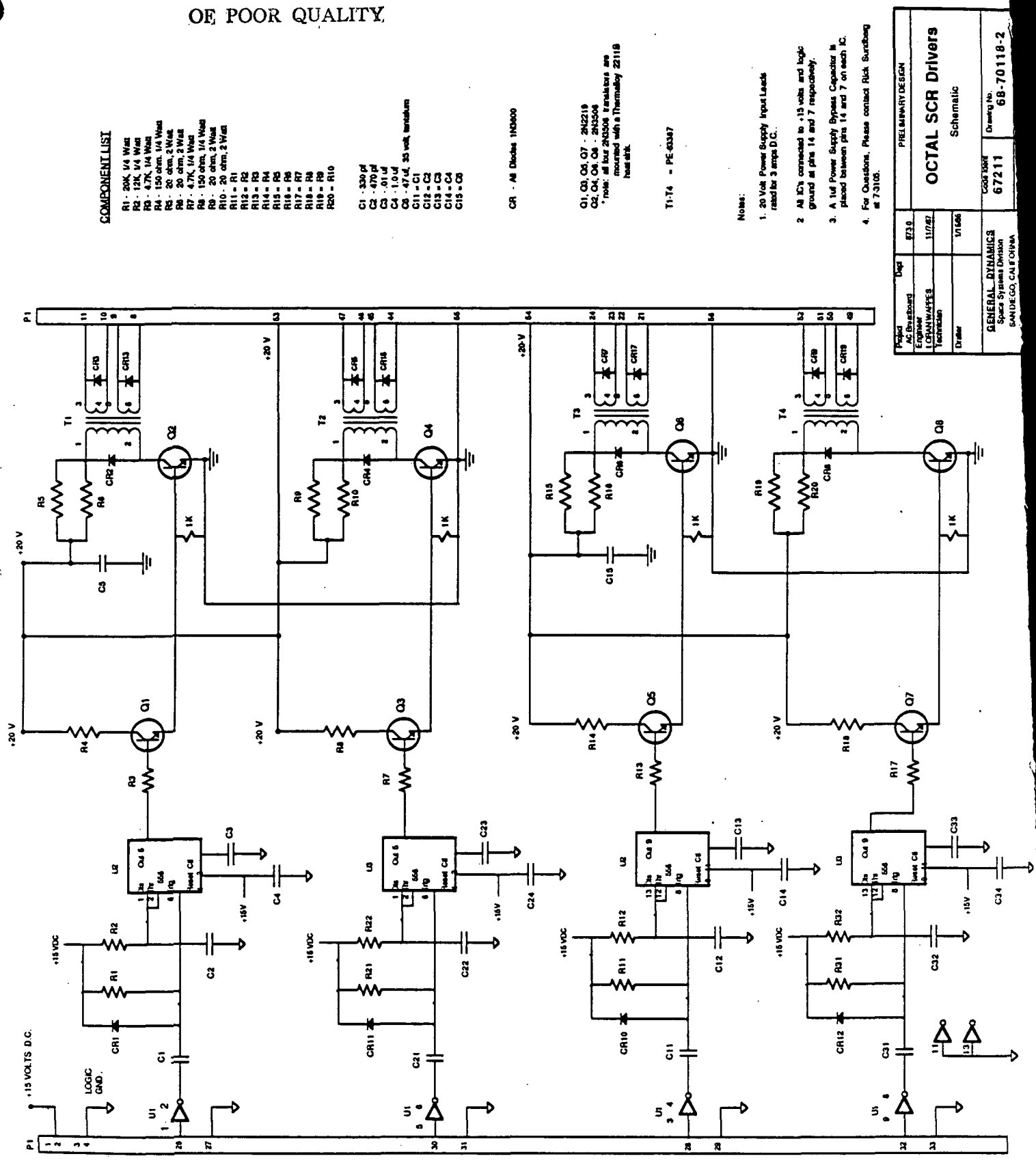


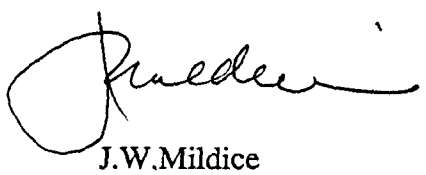
Appendix D

Test Plan

AC Power System Breadboard

Test Plan

NAS 8-36429

Approved by: 

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1. Scope

This test plan provides the requirements for the testing of the AC Power Processing Breadboard designed and constructed by General Dynamics, Space Systems Division, and to be delivered to NASA, Marshall Space Flight Center. It describes the device under test and parameters to be measured. This document is complemented by a formal Acceptance Test Procedure (ATP) document, which describes the instrumentation required, and the detailed steps necessary to verify correct operation of the breadboard, and to satisfy the requirements of this plan. Sucessful completion of the test procedure will constitute satisfaction of the ATP milestone of the breadboard contract.

2. Device Under Test

The device to be tested is a 20 kHz ac power system breadboard (see Figure 1) which uses the resonant ac power approach developed by General Dynamics. The breadboard is representative of a Space Station power system and includes:

- DC or low-frequency to high-frequency conversion
- High voltage and high frequency ac power transmission
- Fault-isolation switches
- Distributed payload power processing
- Computer control

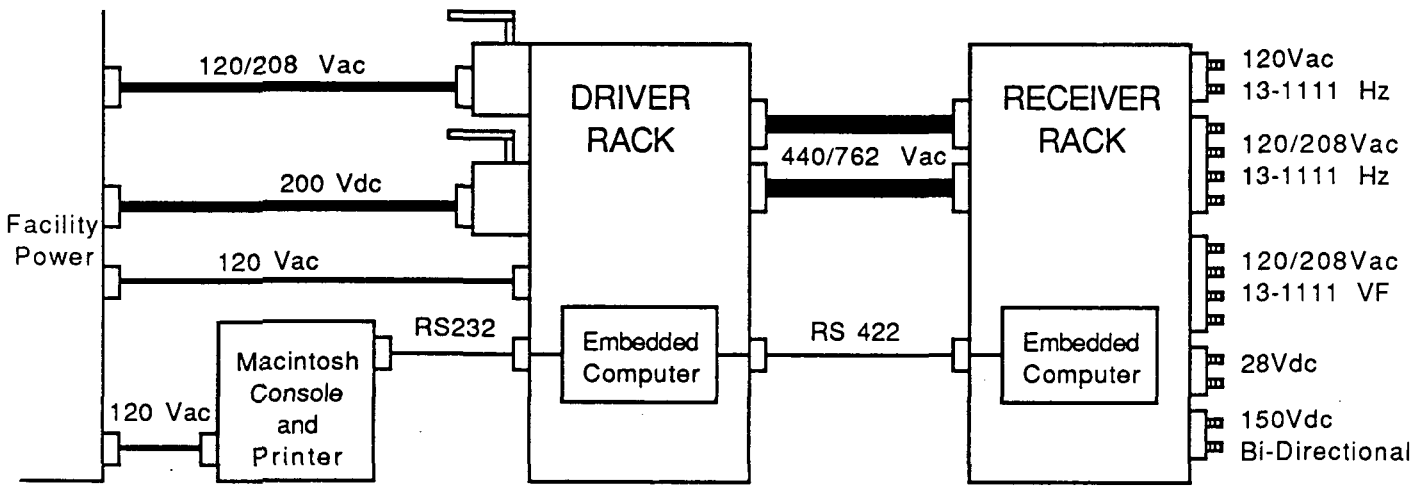

Figure 1. The breadboard to be tested transforms facility power to 20kHz power and then to various other forms of power likely to be required by Space Station users.

The individual modules that make up the breadboard are described below.

Inverters

Nine single-phase, 556W inverter modules are configured to deliver 5 kW to the 20 kHz bus. These driver modules can be operated from either 120/208 Vrms three-phase ac, or 200 Vdc power sources. For each inverter module there is a corresponding transformer that steps up the output of the inverter to the bus voltage (440 Vrms, line to neutral). The inverter, transformer, and bus may be reconfigured so that either single-phase or three-phase power distribution is possible.

The resonant drivers are synchronized to a common clock and operate at 20 kHz. The inverters have closed-loop voltage regulation. The output voltage is sensed and compared to a computer-generated reference voltage to produce an error signal. The error signal is minimized by shifting the phase of two out of three inverters of an inverter triplet in opposite directions, thereby maintaining a constant phase angle in the output waveform.

System Bus

Between the inverter cabinet and the receiver cabinet there are two 50 meter transmission lines. When the breadboard is wired to operate in the three phase mode, each line is made up of three shielded Litz wire conductors which are twisted about themselves. The center conductors carry the line currents, the shields provide the neutral return path. The overall harness is then shielded. When the breadboard is wired in the single phase mode, the three center conductors are paralleled together. The cables have standard MS type connectors on each end, with the conductors soldered into the connector pins. The cables plug into receptacles on the back side of the cabinets. Inside the cabinets, Litz wire conductors are used to route power from the inverters to the back side of the transmission line receptacles.

Switches

Fault-isolation switches are located between the bus and each power module, so that a fault in any module or its transformer can be isolated from the bus. Each switch has fault-detection capability. The control circuitry of each switch monitors the voltage of the bus and current in the module. If both of these parameters exceed a prescribed value, the switch is opened and the module and its transformer are removed from the bus.

Receivers — Five load-interface modules are connected via step-down transformers to the bus at 50 meters from the system drivers. Each of the receiver modules has closed-loop feedback control to regulate output voltage. The output voltage is sensed and compared to a computer-generated reference voltage to produce an error signal. The error signal is minimized by modifying the firing angle of the SCRs.

Computers — The system is controlled by three microcomputers. A Macintosh computer serves as the user interface and supervisory computer. Two Intel single-board computers are imbedded in the hardware, one in the Inverter cabinet, and one in the receiver cabinet. The operator uses the Macintosh to command voltages and currents of the inverter and switch modules, and voltages, currents, and frequencies of the receiver modules. The Macintosh then sends the appropriate commands to the imbedded computers, which use digital-to-analog and digital output boards to interpret these commands and pass them to the hardware. The computers also monitor system voltages and currents, using signal conditioning and analog-to-digital boards, and display them on the Macintosh screen for engineering use when commanded.

3. Requirements

The formal ATP contains very detailed requirements to be met by the hardware. The general requirements are listed in this section.

Inverter	Input: 120/208 Vac, 60 Hz, 3-phase or 200 Vdc
	Output: 440 Vac ±5%, 20 khz ±1%, 3-phase or 1-phase, 5 kW min
Power busses	Share loads under normal operating conditions
	Each bus capable of supplying full load
	Each bus at least 15 meters in length
AC60 receiver	120 Vac, 13-1111 Hz, 1-phase, 1 kW
AC400 receiver	120/208 Vac ±5%, 13-1111 Hz, 3-phase, 1 kW
ACVF receiver	120/208 Vac ±5%, 13-1111 Hz, 3-phase, 1 kW
DC receiver	28 Vdc ±1Vdc, 1 kW
BDC (receiver)	150 Vdc nom, 1kW
BDC (inverter)	Input: 150 Vdc battery
	Output: 440 Vac ±5%, 20 khz ±1%, 3-phase or 1-phase, 1 kW
Switches	Capable of managing inverters, 2 busses, and 5 load modules

	Under control of microprocessor controller
Computers	Include appropriate interfaces for I/O of data for human operator
	Graphic-oriented operator interface program
System	Capable of running with any combination of modules removed
	Allowable power factor 0.8 lag to 0.8 lead
	Capable of running continuously at full power

4. Parameters to be Measured

The following table shows the parameters to be measured, and their acceptable limits.

Module	Parameter	Min Value	Max Value
Inverter	Voltage	418	462
	Frequency (kHz)	19.8	20.2
	Power factor	0.8 lag	0.8 lead
AC60	Voltage	114	126
	Frequency (Hz)	-1% of Cmd.	+1% of Cmd.
AC400	Voltage	114	126
	Frequency (Hz)	-1% of Cmd.	+1% of Cmd.
ACVF	Voltage	114	126
	Frequency (Hz)	-1% of Cmd.	+1% of Cmd.
DC	Voltage	27	29
BDC	Voltage	150 Nom	150 Nom

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